ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)

Vol 8, Issue 3, March 2021

Design of 4x4 Reversible Multiplier using Reversible TSG Gate

[1] Veena Durgam, [2] Dr. K. Ragini, [3] Divya Durgam

[1][3] M.Tech Student, Department of Electronics and Communication (DECE), G. Narayanamma Institute of Technology and Science, Shaikpet, Hyderabad, India

[2] Professor, Department of Electronics and Communication (DECE), G. Narayanamma Institute of Technology and Science, Shaikpet, Hyderabad, India

Email: [1] durgamveena955@gmail.com, [2] ragini.kanchimi2011@gmail.com, [3] durgamdivya1996@gmail.com

***Abstract*--- Multipliers are very important components of any processor or computing machine. The performance of microcontrollers and Digital signal processors are evaluated based on the number of multiplications performed in a unit of time. Hence better multiplier architectures are assured to increase the efficiency of the system. The reversible multiplier is one such promising solution. In this paper, a 4x4 reversible unsigned multiplier is being designed. The Fredkin gates (FRG) are used for producing the partial products and Thapliyal Srinivas Gate (TSG) singly can be used as a half adder and as a full adder for the addition of partial products. The design is implemented using Xilinx ISE 14.7 design suite.**

***Keywords*--- Reversible logic gates, reversible logic circuits, reversible multipliers, Constant Input, Delay, Garbage Output, Quantum Cost**

I. INTRODUCTION

The most important basic function in arithmetic operations is multiplication. Presently these are used in many Digital Signal Processing (DSP) applications such as Fast Fourier Transform (FFT), convolution, filtering, and microprocessors in its arithmetic and logic unit. There is a need for a high-speed multiplier since multiplication dominates the execution time of most DSP algorithms. The demand for high-speed processing has been increasing, as a result of expanding computer and signal processing applications. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuits has been a subject of interest over decades. Reducing the time delay and power consumption are very important requirements for many applications.

In today's world, designing a Low power circuit is one of the most interesting topics in current researches. However, device scaling is critically limited by power dissipation, demanding better power optimization methods. According to Bennet et al [5], irreversible circuits result in heat dissipation as a result of bit loss. KTln2 Joules of energy is wasted for each bit of information loss [4], where K is the Boltzmann constant and T is the absolute temperature. Hence reversible circuits should be constructed to minimize energy dissipation and data loss.

Reversible computation is very important in the field of quantum computing, bioinformatics, nanotechnology, optical com- putting, information security, digital signal processing, low-power complementary metal-oxide-semiconductor (CMOS) design, quantum-dot cellular automata, etc. [6].

In this paper, an efficient multiplication algorithm has been proposed which explains the multiplication of two 4-bit numbers. The reversible multiplier circuit has been designed using the proposed algorithm. It uses 16 Fredkin gates (FRG) for partial product generation and 13 TSG gates are used as half adder and full adder for the addition of partial products.

The paper is organized as follows: Section II introduces the preliminaries; Section III presents the best-known works; Section IV presents the Related work, Section V discusses the proposed circuit, the proposed design is compared with the existing multipliers in Section VI and the paper is concluded in Section VII.

II. PRELIMINARIES

In this section, the basic definitions and properties required to present our proposed methodologies are explained.

Quantum cost: The quantum cost of a reversible gate is the number of primitive reversible logic gates used in the circuit.

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)

Vol 8, Issue 3, March 2021

Constant input: The number of inputs that are to be maintained constant to preserve the reversibility of the reversible gates.

Garbage output: The outputs that are neither used as input nor as output for further computations are called garbage outputs of the circuit.

Hardware complexity: It is defined as the number of logic operations performed by the circuit. The total logical calculation is the count of the Ex-OR (α), AND (β), and NOT (δ) in the output expressions of the circuit.

Delay: The number of gates used in the critical path from input to output of the circuit.

III. BASIC REVERSIBLE LOGIC GATES

Several 3x3 reversible gates such as the Toffoli gate and the Peres gate have been reported in the literature. Each reversible gate has a cost associated with it called the quantum cost. The quantum cost of a reversible gate is the number of 1x1 and 2x2 reversible gates or quantum logic gates required in its design. The quantum costs of all the reversible 1x1 and 2x2 gates are taken as unity. Any reversible gate can be realized using the 1x1 NOT gate, and 2x2 reversible gates such as Controlled-V and Controlled-V + (V is a square-root-of NOT gate and V + is it's hermitian) and the Feynman gate which is also known as the Controlled NOT gate (CNOT). Thus, the quantum cost of a reversible gate can be calculated by counting the numbers of NOT, Controlled-V, Controlled-V +, and CNOT gates required in its implementation. The basic reversible logic gates encountered during the design are listed below:

A) The NOT Gate:

A NOT gate is a 1x1 gate represented as shown in Fig. 3.1. Since it is a reversible 1x1 gate, its quantum cost is unity.

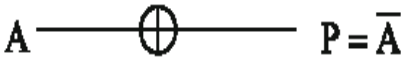


Fig. 3.1: NOT gate

B) The Controlled-V and Controlled-V + Gates:

The controlled-V gate is shown in Fig. 3.2. In a controlled-V gate, when the control signal A=0, then the qubit B will pass through the controlled part without change, i.e., we will get Q=B. When A=1 then the unitary operation V = i+1 2 1 −i −i 1 is applied to the input B, i.e., Q=V(B). The controlled-V + gate is shown in Fig. 3.3. In the controlled-V + gate when the control signal A=0 11 then the qubit B will pass through the controlled part unchanged, i.e., we will have Q=B. When A=1 then the unitary operation V + = V −1 is applied to the input B, i.e., Q=V +(B). The V and V + quantum gates have the following properties: V × V = NOT, V × V + = V + × V = I V + × V + = NOT. The properties above show that when two V gates are in series they will behave as a NOT gate. Similarly, two V + gates in series also function as a NOT gate. A V gate in series with V + gate, and vice versa, is an identity.

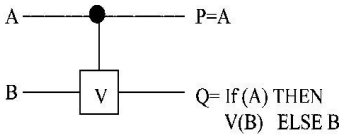


Fig. 3.2: The Controlled -V gate

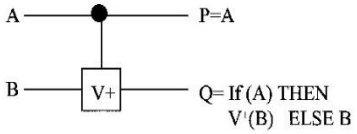


Fig. 3.3: The Controlled- V+ gate

C) The Feynman Gate (CNOT Gate):

The Feynman gate (FG) or the Controlled-NOT gate (CNOT) is a 2x2 reversible gate having mapping (A, B) to (P=A, Q=A⊕B) where A, B are the inputs and P, Q are the outputs, respectively. Since it is a 2x2 reversible gate, it has a quantum cost of 1. Figures 3.4(a) and 3.4(b) show the block diagram and quantum representation of the Feynman gate. The Feynman gate can be used for copying the signal thus avoiding the fanout problem in reversible logic as shown in Fig. 3.4(c). The circuit of the Feynman gate is shown in Fig. 3.4(d).

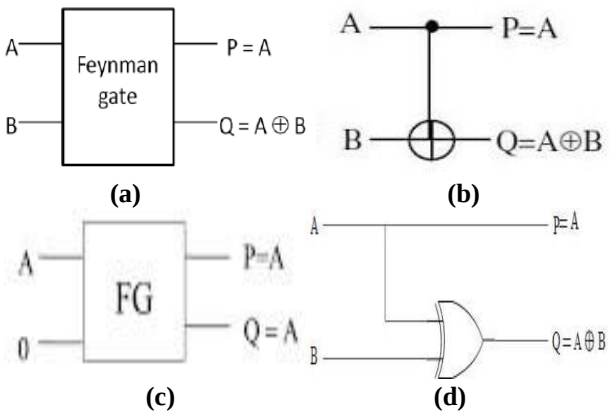


Fig. 3.4: (a) Feynman gate, (b) Quantum representation, (c) Feynman gate for avoiding the fanout, (d) Circuit diagram

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)

Vol 8, Issue 3, March 2021

D) The Toffoli Gate:

The Toffoli gate (TG) is a 3x3 reversible gate having the mapping (A, B, C) to (P=A, Q=B, R=AB⊕ C), where A, B, C are the inputs and P, Q, R are the outputs, respectively as shown in Fig. 3.5(a). The Toffoli gate is one of the most popular reversible gates and has a quantum cost of 5 as shown in Fig. 3.5(b). The circuit diagram of the Toffoli gate is shown in Fig. 3.5(d). The quantum cost of this gate is 5 as it needs 2V gates, 1 V + gate, and 2 CNOT gates to implement it. The Toffoli gate can also be used as an AND gate as shown in Fig. 3.5(c).

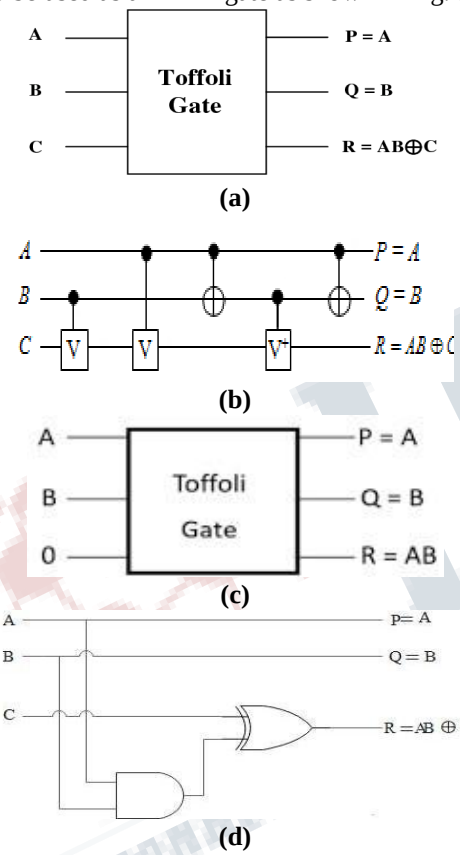


Fig. 3.5: (a) Toffoli gate, (b) Quantum representation, (c) Toffoli gate as AND gate, (d) Circuit diagram

E) The Peres Gate:

The Peres gate is a reversible 3x3 gate as shown in Fig. 3.6(a) having the mapping (A, B, C) to (P=A, Q=A⊕B, R= A·B⊕C), where A, B, C are the inputs and P, Q, R are the outputs respectively. Fig. 3.6(b) shows the quantum implementation of the Peres gate (PG) with a quantum cost of 4, and Fig. 3.6(d) shows the circuit diagram of the Peres gate, respectively. The quantum cost of the Peres gate is 4 since it requires 2 V gates, 1 V+ gate, and 1 CNOT gate in its design. In the existing literature, among the several 3x3 reversible gates, the Peres gate has the minimum quantum cost. The Peres gate can also be used as a half adder and "AND" gate as shown in Fig. 3.6(c).

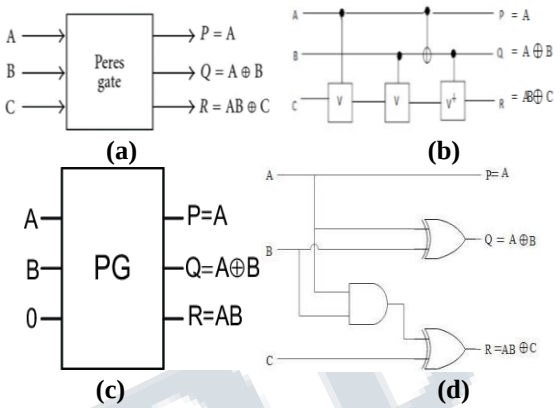


Fig. 3.6: (a) Peres gate, (b) Quantum representation, (c) Peres gate as half adder & AND gate, (d) Circuit diagram F) Fredkin Gate (FRG):

The Fredkin gate (TG) is a 3 inputs 3 outputs (3x3) reversible gate having the mapping (A, B, C) to (P=A, Q=$\bar{A}$B⊕AC, R= AB⊕$\bar{A}$C), where inputs are A, B, C and outputs are P, Q, R respectively. Fig. 3.7(a) shows the Fredkin gate, Fig. 3.7(b) shows the quantum implementation of the Fredkin gate (FRG) with a quantum cost of 5, and Fig. 3.7(d) shows the circuit diagram of the Fredkin gate, respectively. The quantum cost of the Fredkin gate is 5 since it requires 2 V gates, 1 V+ gate, and 4 CNOT gates in its design. The Fredkin gate can also be used as an AND gate as shown in Fig. 3.7(c).

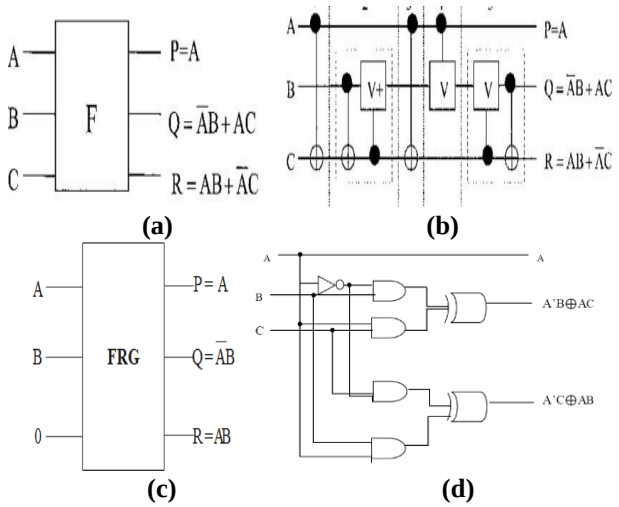


Fig. 3.7: (a) Fredkin gate, (b) Quantum representation, (c) Fredkin gate as AND gate, (d) Circuit diagram

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)

Vol 8, Issue 3, March 2021

G) Thapliyal Srinivas Gate (TSG):

The TSG gate is a 4 inputs 4 outputs (4x4) reversible gate having the mapping (A, B, C, D) to (P=A, Q=A'C'⊕B',R=(A'C'⊕B')⊕D,S=(A'C'⊕B')D⊕AB⊕C), where A, B, C are the inputs and P, Q, R are the outputs respectively. Fig. 3.8(a) shows the Thapliyal Srinivas gate (TSG), Fig. 3.8(b) shows the quantum implementation of the Thapliyal Srinivas gate (TSG) with the quantum cost of 17, and Fig. 3.8(d) shows the circuit diagram of Thapliyal Srinivas gate, respectively. The quantum cost of the Thapliyal Srinivas gate is 17 since it requires 8 V gates, 3 V+ gates, and 9 CNOT gates in its design. The Thapliyal Srinivas gate can also be used as a half adder and "AND" gate as shown in Fig. 3.8(c).

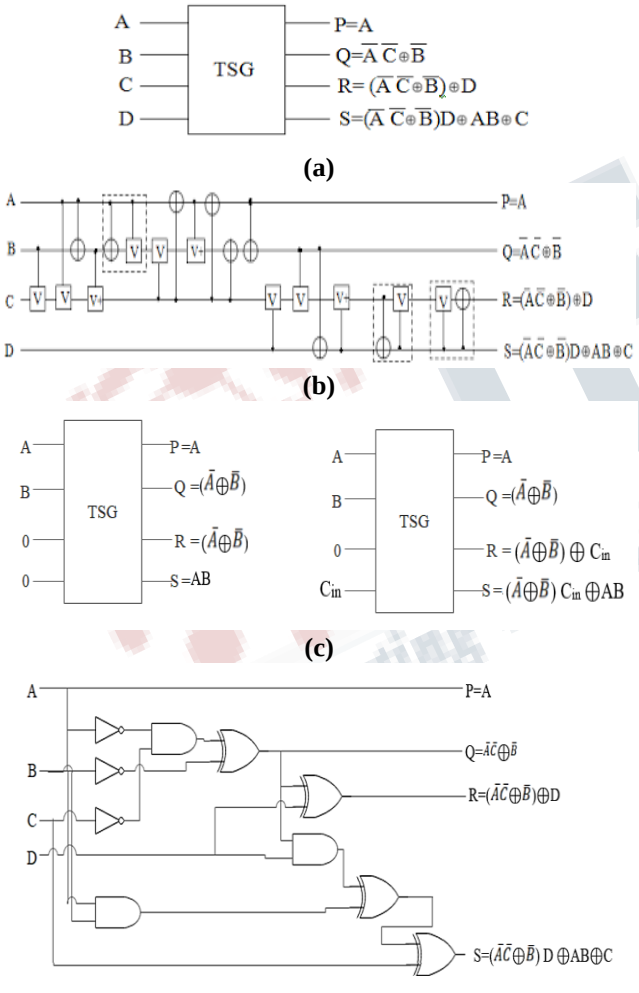


Fig. 3.8: (a) Thapliyal Srinivas gate (TSG), (b) Quantum representation, (c) Thapliyal Srinivas gate as half adder and Full adder, (d) Circuit diagram

IV. RELATED WORK

In existing literature work, there are different designs of Multiplier circuits developed and designed using reversible gates. Multipliers have special importance because they can significantly affect the performance of digital systems. Due to this fact, extensive research has been carried out to reduce the circuit delay, quantum cost, constant inputs, garbage outputs, respectively. Generally, the multipliers can be designed in a serial or parallel manner. When the low–cost design is considered, serial multipliers are very important. On the other hand, if the high-speed design is aimed at, parallel multipliers are desirable. Also, multipliers can be unsigned and signed. In the following, previous parallel unsigned reversible multipliers are reviewed with different reversible gates, and each of them has its advantages and disadvantages.

In 1961, R. Landauer [4] described that logical irreversibility is associated with physical irreversibility and requires a minimal heat generation per machine cycle. For irreversible logic computations, each bit of information lost generates kTlog2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. In a conventional system, millions of gates are used to perform logical operations. The author proved that heat dissipation avoidable if the system is made reversible.

In 1973, C.H. Bennett [5] described that if a computation is carried out in Reversible logic zero energy dissipation is possible, as the amount of energy dissipated in a system is directly related to the number of bits erased during computation. The design that does not result in information loss is irreversible. A set of reversible gates are needed to design a reversible circuit. A reversible gate can generate a unique output vector from each input vector and vice versa.

H. Thapliyal and M.B Srinivas [1] provided a reversible multiplier circuit in which FG gate is used for generating the partial product bits, and Thapliyal- Srinivas gate (TSG) is applied as full-adder in summation network. The reversible multiplier circuit is implemented using Xilinx ISE 9.1 design suite. Simulation results depict the design has a quantum cost of 274, 58 garbage outputs, 46 constant inputs and it achieved 11ns of delay.

In 2008, M. Shams, M. Haghparast, and K. Navi [9] used PG and MKG gates to construct the reversible multiplier so that PG is utilized to generate the partial products and MKG is applied as full-adder in summation network. The results of this circuit depict the design has less quantum cost of 232, 56 garbage outputs, 44 constant

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)

Vol 8, Issue 3, March 2021

inputs as compared to the previous design but the delay achieved is the same.

M. Haghparast, M. Mohammadi, K. Navi et al [3] introduced two reversible unsigned multiplier designs which the first design of the HNG and the second design of PFAG as full-adder are used in their summation network. The simulation results of the two designs depict that the designs have the same no. of garbage outputs and constant inputs of 28, quantum cost of design 1 is 137, and design 2 is 153. The circuit has achieved a delay of 11ns of design, 16ns of design 2. The circuits have less no. of quantum cost, garbage outputs, and constant inputs than the previous design but the delay achieved by the two designs are not acceptable as they affect the system performance.

In 2009, M.S. Islam, M. Rahman, Z. Begum et al [16] provided a reversible multiplier using their proposed Peres Full Adder gate (PFAG) as full-adder and PG gate as half-adder in the summation network. They also generated the partial products using a network of PG gates. The measurement results obtained from this circuit have less no. of quantum cost of 144, 52 garbage outputs, 28 constant inputs, and delay as 11ns same as the previous design.

M. Ehsanpour et al, P. Moallem, and A. Vafaei [11] proposed a new reversible gate called Modified Full Adder (MFA) and used it in the summation circuit of a reversible multiplier. They also applied PG gate for generating the partial product bits. The author has shown that his multiplier has 36 garbage outputs, 20 constant inputs compared to the previous designs. The simulation results were carried out by using Xilinx ISE 9.1 design suite.

V. PROPOSED REVERSIBLE MULTIPLIER

The operation of a 4x4 reversible multiplier is depicted in Fig. 5.1. It includes two steps to perform the multiplication of two numbers.

Step 1: Partial Product Generation

Step 2: Addition of Partial Products

			×	x_3	x_2	x_1	x_0
				y_3	y_2	y_1	y_0
				x_3y_0	x_2y_0	x_1y_0	x_0y_0
			x_3y_1	x_2y_1	x_1y_1	x_0y_1	
		x_3y_2	x_2y_2	x_1y_2	x_0y_2		
	x_3y_3	x_2y_3	x_1y_3	x_0y_3			
P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

Fig. 5.1: The operation of the 4x4 multiplier

In the first step, it uses 16 Fredkin gates for the generation of partial products. In the second step, the addition of partial products is done by using Thapliyal Srinivas Gate (TSG) gate as a half adder and as a full adder, as shown in Fig8(c). The structure of the 4x4 reversible multiplier circuit using reversible TSG gate is shown in Fig. 5.1 and Fig. 5.2.

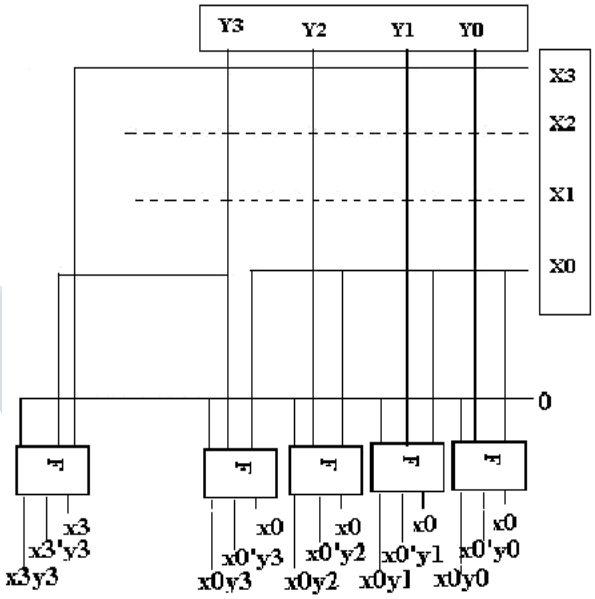


Fig. 10: Partial Products generation circuit using Fredkin gate

In the above circuit, the multiplicand [x] and multiplier [y] are two 4-bit inputs of Fredkin gates (PG) to perform multiplication, the third input of the Fredkin gate is kept as constant 0 to preserve the functionality of the reversible gates. The outputs produced by Fredkin gates are the partial products, and there are also few garbage outputs generated by Fredkin gates that are not used for further computations.

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)

Vol 8, Issue 3, March 2021

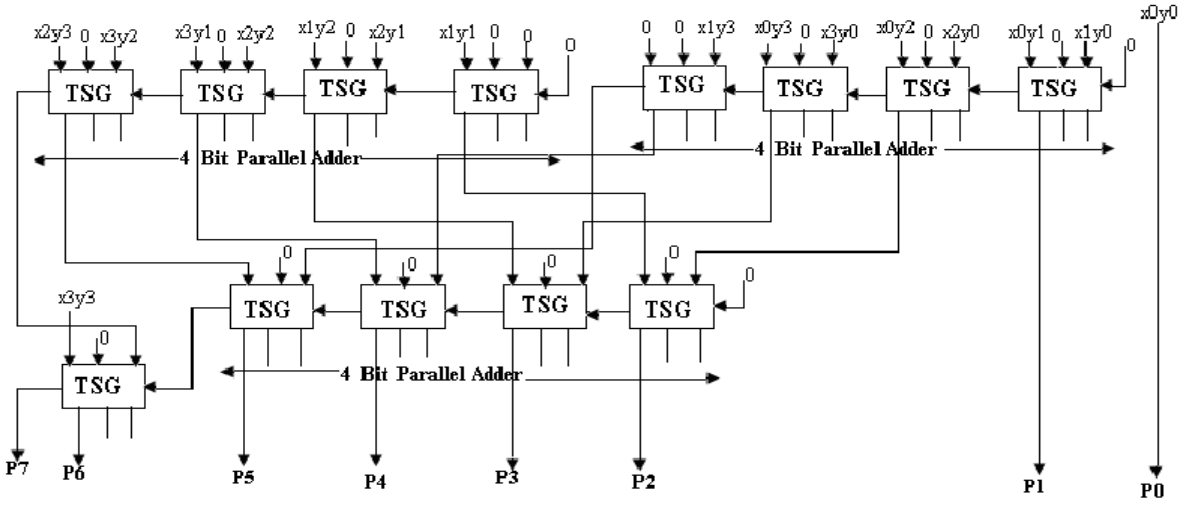


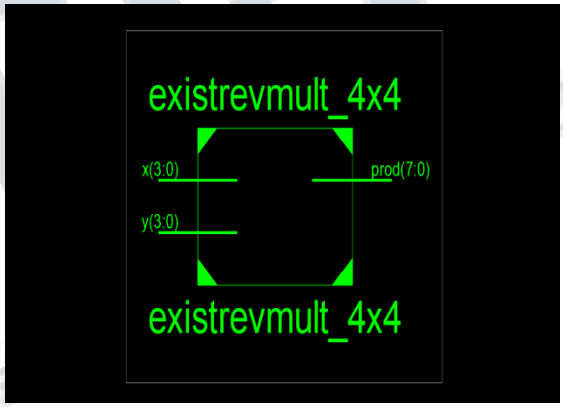
Fig. 5.2: The 4x4 reversible multiplier circuit using TSG gate

The summation circuit of the 4x4 reversible multiplier circuit using reversible TSG gate is shown in Fig. 5.2. Partial products generated in Fig. 10 are added by using the Thapliyal Srinivas gate (TSG). The Thapliyal Srinivas gate is used as a reversible full adder and reversible half adder. To perform the addition operation of partial products, the three partial products are grouped and fed to a reversible full adder, and the two partial products are grouped and fed to a reversible half adder. If only one partial product remains, it will move to the next layer. The inputs to TSG gates are partial products, and the outputs of these gates are final products. There are also few outputs generated by TSG gates that are not used for further computations called garbage outputs.

VI. RESULTS AND DISCUSSIONS

The proposed 4x4 reversible multiplier circuit is designed in Verilog coding using Xilinx 14.7 software. The proposed reversible multiplier circuit is more efficient than the existing multiplier using HNG and PG gates. To present a fair comparison, in TABLE I, we have shown results of different reversible gates and in TABLE II shown results of the existing reversible multiplier circuit our proposed circuit in terms of the number of garbage outputs, constant inputs, quantum cost, and delay.

Fig. 6.1 and Fig. 6.2 show the RTL schematic and simulation results of the proposed reversible 4x4 reversible multiplier circuit.



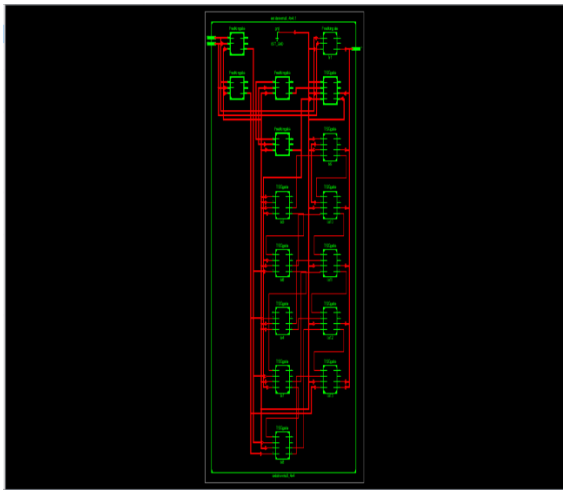


Fig. 6.1: RTL Schematic of existing 4x4 reversible multiplier circuit using TSG gate

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)

Vol 8, Issue 3, March 2021

Fig. 6.2: Simulation results of existing 4x4 reversible multiplier circuit using TSG gate

TABLE I: Comparison of Various Reversible Gates

REVERSIBLE GATES	No. of inputs	No. of outputs	Quantum cost	Delay (ns)
Peres gate (PG)	3	3	4	5.385
Fredkin gate (FRG)	3	3	5	5.456
Thapliyal Srinivas gate (TSG)	4	4	17	5.473
Toffoli gate (TG)	3	3	5	5.776

TABLE Ⅱ: Comparative experimental results of different reversible multiplier circuits.

parameters	Reversible multiplier circuit using PG and HNG gates [2]	Proposed reversible multiplier circuit using TSG gate and FRG gate
No. of constant inputs	28	34
No. of garbage outputs	52	58
Total Quantum cost	140	221
Delay(ns)	11.91	10.422

VII. CONCLUSION

In this work, we have proposed a reversible 4x4 multiplier using TSG and FRG gates. It is designed in Verilog coding using Xilinx 14.7. It is observed from the results that the proposed reversible multiplier has less delay compared to the existing reversible multiplier [2]. Future work includes further attempts at minimizing total multiplier cost, ancilla inputs, and garbage outputs. And of course, reduction in the delay is also a critical area of study in upcoming years.

REFERENCES

[1] H. Thapliyal, and M. Srinivas, "Novel reversible multiplier architecture using reversible TSG gate."

[2] M. Haghparast, S. J. Jassbi, K. Navi, et al., “Design of a novel reversible multiplier circuit using HNG gate in nanotechnology,” World Appl. Sci. J, vol. 3, no. 6, pp. 974- 978, 2008.

[3] M. Haghparast, M. Mohammadi, K. Navi, et al., “Optimized reversible multiplier circuit,” Journal of Circuits, Systems, and Computers, vol. 18, no. 02, pp. 311-323, 2009.

[4] R. Landauer, "Irreversibility and heat generation in the computing process," IBM journal of research and development, vol. 5, no. 3, pp. 183-191, 1961.

[5] C. H. Bennett, "Logical reversibility of computation," IBM journal of research and development, vol. 17, no. 6, pp. 525-532, 1973.

[6] M. Perkowski, L. Jozwiak, P. Kerntopf, et al., "A general decomposition for reversible logic." pp. 119-138.

[7] M. Perkowski, and P. Kerntopf, "Reversible Logic. Invited tutorial."

[8] H. Thapliyal, and M. Srinivas, "A novel reversible TSG gate and its application for designing reversible carry look-ahead and other adder architectures." pp. 805-817.

[9] M. Shams, M. Haghparast, and K. Navi, “Novel reversible multiplier circuit in nanotechnology,” World Appl. Sci. J, vol. 3, no. 5, pp. 806-810, 2008.

[10] P. Kerntopf, M. A. Perkowski, and M. H. Khan, "On the universality of general reversible multiple-valued logic gates." pp. 68-73.

[11] M. Ehsanpour, P. Moallem, and A. Vafaei, "Design of a novel reversible multiplier circuit using modified full adder." pp. V3-230-V3-234.

[12] W. C. Athas, and L. Svensson, "Reversible logic issues in adiabatic CMOS." pp. 111- 118.

[13] T. Toffoli, “Reversible Computing” Tech memoMIT/LCS/TM-151, MIT Lab for Computer Science 1980.

[14] Fredkin E. Fredkin and T. Toffoli, "Conservative Logic", Int'I J. Theoretical Physics Vol 21, pp.219-253, 1982.

[15] Peres, "Reversible Logic and Quantum Computers", Physical Review A, 32:3266-3276, 1985.

[16] M. S. Islam, M. Rahman, Z. Begum, et al., "Low-cost quantum realization of reversible multiplier circuit," Information technology journal, vol. 8, no. 2, pp. 208-213, 2009.