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Simulation and Comparative Analysis of Multi-Gate Silicon Nanowire Field Effect Transistor

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Abstract: In this paper, we present the simulation of silicon nanowire field effect transistor (SNW FETs) with multiple gates. The simulation of SNW FETs with multiple gates such as top-gate, double-gate, tri-gate, pi-gate, omega-gate and Gate-all-around gate structures are performed based on Current-Voltage (I-V) characteristics using Nanohub Multi-gate Nanowire FET simulator. Simulation studies are performed based on Current Voltage characteristics of Multi gate Nanowire FET. Effects of varying oxide thickness in multiple gates are also presented.

Index Terms— Field effect transistor, I-V characteristics, Multi gate Nanowire FET, Gate all around, OFF current

I. INTRODUCTION

The rise of new technology continues from the scaling of MOSFET devices to extending CMOS down to even smaller technology node. Yet the scaling of CMOS device has strayed from the the scaling rules set out by Dennard et al.[1] and patterns predicted by Moore [2] because of fundamental physical and technical limitations. The major concern is that the CMOS scaling in to atomic dimension is slowing down due to certain limitations like leakage current, channel length modulation and heat dissipation. Hence, new semiconductor technology needs to be developed immediately to solve the problems like power dissipation, reliability, speed, cost etc.. Due to continuous efforts and out of all, Nano electronics emerged as one of most encouraging solutions towards CMOS device scaling.

The flow of holes and electrons between the source and drain contacts are controlled by a gate electrode in all modern transistors. In CMOS transistors, this modulation depends on the existence of a junction between the channel and the source and drain contacts. With the shrinking dimensions of modern transistors, creating these junctions is becoming more problematic [3]. The first patented field effect transistor, suggested by Julius Edgar Lilienfeld in the 1920's was a junction-free device. It was designed such that charge carriers could be depleted by the actions of the gate. However, to be able to fully turn off the device, a very thin nanoscale channel (nanowire) is necessary.

As we continuously shrinking the transistors, gate cannot control the leakage paths that are far away from the gates. Providing gate control from more than one side of the channel is a way to eliminate the leakage paths. So, Single gate MOSFETs has evolved from single gate to multiple gates such as double-gate, tri-gate, and gate all around as shown in Fig.1. In Multi-gate FET, the gate has great control over the channel region, thus providing a better electrostatic integrity.

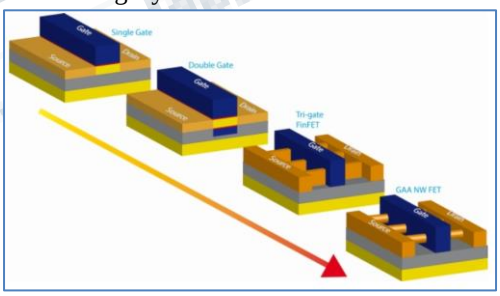

Figure 1. Progression of FETs form Single gate to Gate all around

The objective of this paper is to hypothetically examine the fundamental properties of Silicon Nanowire Field Effect transistors and its Current Voltage characteristics. The browser based simulations are done utilizing 3D test system for silicon nanowire FET with different gates accessible at www.nanohub.org

II. LITERATURE REVIEW

In ref [5], the authors discuss about the tri-gate CMOS transistor experimental results with physical gate lengths Lg = 60 nm. The devices displayed full depletion with silicon body thickness, T_{si} = 36 nm approximately 2 times

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that required for single gate and Silicon body width , W_{si} = 55 nm approximately 1.5 times that required for double gate device. The tri gate CMOS transistor, for 3D simulations with gate length (L_g) = body thickness (T_{Si}) = body width (W_{Si}) = 30 nm, maintains full depletion and exhibit excellent short channel performance. The Author suggested that, in near future, bulk CMOS transistor could be replaced by this transistor design.

In ref [6], the author presented double-gate, tri-gate and gate all around MOSFETs in various forms for compact energy quantization modeling using closed-form analytical solutions of Poisson and Schrodinger equations. For three types of MOSFETs, charge density, lowest sub band energy, drain current was investigated in detail and it is clearly evident that surrounding gate MOSFETs has additional advantage with respect to double-gate, tri-gate devices.

III. SILICON NANOWIRE FET STRUCTURE

The 3D Silicon Nanowire FET structure in use for simulation is as shown in Fig.2. The Two dimensional structure of Nanowire FET is shown in Fig.3 and cross sections of different gates is shown in Fig.4. The Table 1 shows the several parameters and their values used in simulation of Silicon multi gate Nanowire FETs.

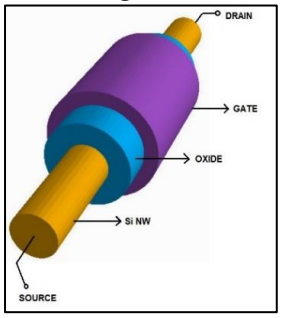

Figure 2. 3D Structure of Silicon Nanowire

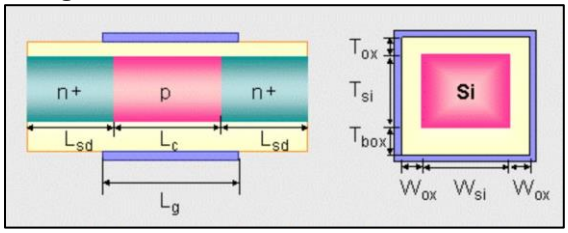

Figure 3. Two Dimensional Structure of Silicon Nanowire Transistor used in simulation.

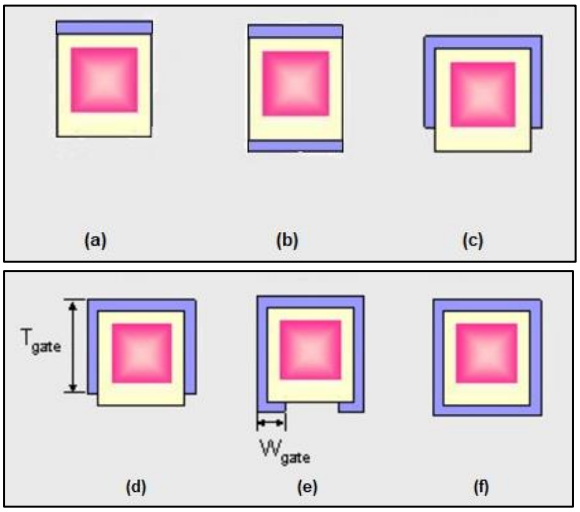

Figure 4. Sectional View of Different gates (a) Top Gate (b) Double-gate (c) Tri-gate (d) Pi-gate (e) Omega-gate (f) Gate All Around

Table 1: Device parameters for silicon based multi gate nanowire FET.

S.No.	Parameters	Symbol	Values
1	Source/Drain length	L_{sd}	10 nm
2	Channel length	L_c	10 nm
3	Gate length	L_g	10 nm
4	*Oxide thickness*	T_{ox}	*1 nm, 2 nm, 3 nm*
5	Silicon oxide thickness	T_{si}	5 nm
6	Buried oxide thickness	T_{box}	1 nm
7	Oxide width	W_{ox}	1 nm
8	Silicon body width	W_{si}	5 nm
9	Tgate (for pi gate)	-	7 nm
10	Wgate (for Omega gate)	-	3 nm
11	Temperature	T	300 K
12	Silicon bandgap	E_g	1.12 eV
13	Si dielectric constant	ε_{Si}	11.9
14	Si work function	ϕ_{Si}	4.05 eV
15	Silicon orientation	(x,y,z)	1, 0, 0
16	Oxide bandgap	E_{ox}	9 eV
17	Oxide dielectric constant	ε_{ox}	3.9

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18	Oxide effective mass	m_{eff}	0.5 m0
19	Gate work function	ϕ_G	4.61eV
20	Channel doping density	N_{ch}	$1.0\times e^{15}$ cm-3
21	Silicon doping density	N_{sd}	$1.0\times e^{20}$ cm-3

IV. SIMULATION RESULTS

In this work, we are presenting about the different type of gates as shown in fig.3 i.e. Top gate, Double gate, Tri gate, Pi gate, Omega gate and Gate all around. For each type of gate, simulations are done with different oxide thickness i.e. 1 nm, 2nm & 3nm. These are simulated using Nano hub tool which is a browser simulation stand-alone tool. The simulations results for different gate types with varying oxide thickness from 1 nm to 3 nm is presented below

4.1 Top gate: As seen in Fig. 5(a), for top gate with oxide thickness of 1 nm, the OFF current (Ioff) is $5.03e^{-8}$ A and ON current (Ion) is $2.00e^{-5}$ A. The leakage current decreases with decrease in oxide thickness.

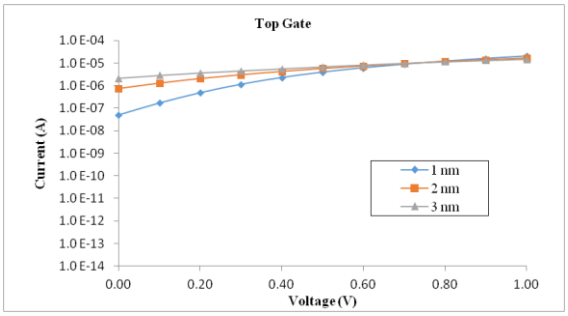

Figure 5(a). I-V characteristics for top gate with different oxide thickness

4.2 Double gate: As seen in Fig. 5(b), for Double gate with oxide thickness of 1 nm, the OFF current (Ioff) is $4.36e^{-14}$ A and ON current (Ion) is $4.04e^{-5}$ A. The leakage current decreases with decrease in oxide thickness. With Comparison with top gate, the OFF current (Ioff) is lower for the double gate but the ON current (Ion) remains almost same for the both the gates.

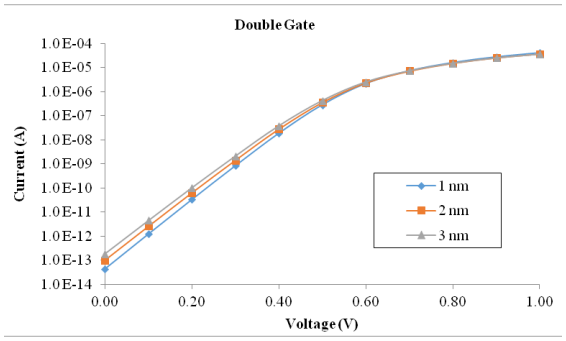

Figure 5(b). I-V characteristics for double gate with different oxide thickness

4.3 Tri gate: As seen in Fig. 5(c), for Tri gate with oxide thickness of 1 nm, the OFF current (Ioff) is $5.64e^{-13}$ A and ON current (Ion) is $3.39e^{-5}$ A. The leakage current decreases with decrease in oxide thickness. With Comparison with top gate, the OFF current (Ioff) is lower for the Tri gate but higher than Double gate.

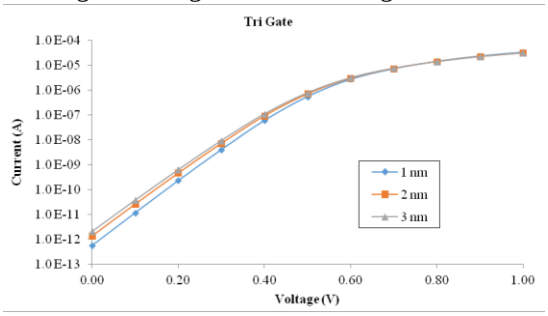

Figure 5(c). I-V characteristics for Tri gate with different oxide thickness

4.4 Pi gate: As seen in Fig. 5(d), for Pi gate with oxide thickness of 1 nm, the OFF current (Ioff) is $3.63e^{-13}$ A and ON current (Ion) is $3.46e^{-5}$ A. Similarly for Pi gate also the leakage current decreases with decrease in oxide thickness.

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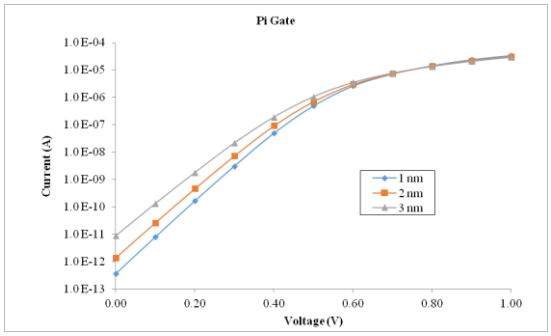

Figure 5(d). I-V characteristics for Pi gate with different oxide thickness

4.5 Omega gate: As seen in Fig. 5(e), for Omega gate with oxide thickness of 1 nm, the OFF current (Ioff) is $4.36e^{-14}$ A and ON current (Ion) is $4.04e^{-5}$ A and the leakage current decreases with decrease in oxide thickness. For Omega gate the OFF Current and ON Current Values are same as of Double gate.

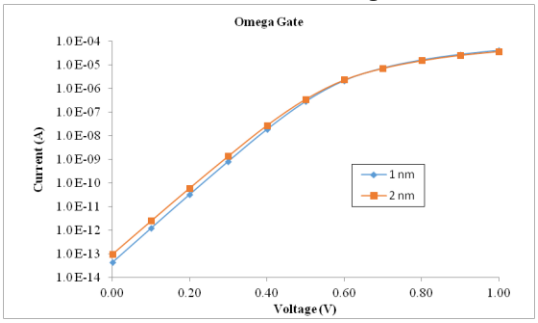

Figure 5(e). *I-V characteristics for Omega gate with different oxide thickness*

4.6 Gate all around: As seen in Fig. 5(f), for Gate all around with oxide thickness of 1 nm, the OFF current (Ioff) is $3.84e^{-14}$ A and ON current (Ion) is $4.10e^{-5}$ A and the leakage current decreases with decrease in oxide thickness.

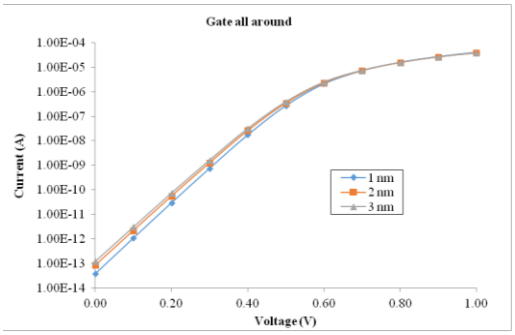

Figure 5(f). I-V characteristics for Gate all around with different oxide thickness

Table 2. OFF Current and ON Current Values for different Oxide thickness

S. No.	Type of gate	OFF Current (Ioff) - A			ON Current (Ion) - A		
		1nm	2nm	3nm	1nm	2nm	3nm
1	Top Gate	$5.03e^{-08}$	$7.55e^{-07}$	$2.15e^{-06}$	$2.00e^{-05}$	$1.64e^{-05}$	$1.50e^{-05}$
2	Double gate	$4.36e^{-14}$	$9.98e^{-14}$	$1.85e^{-13}$	$4.04e^{-05}$	$3.75e^{-05}$	$3.58e^{-05}$
3	Tri Gate	$5.64e^{-13}$	$1.40e^{-12}$	$2.07e^{-12}$	$3.39e^{-05}$	$3.13e^{-05}$	$3.12e^{-05}$
4	Pi Gate	$3.63e^{-13}$	$1.40e^{-12}$	$8.84e^{-12}$	$3.46e^{-05}$	$3.13e^{-05}$	$2.92e^{-05}$
5	Omega Gate	$4.36e^{-14}$	$9.72e^{-14}$	-	$4.04e^{-05}$	$3.75e^{-05}$	-
6	Gate all around	$3.84e^{-14}$	$8.53e^{-14}$	$1.22e^{-13}$	$4.10e^{-05}$	$3.81e^{-05}$	$3.72e^{-05}$

From Table 2, Out of all type of gates, Gate all around has lowest OFF current (Ioff) values and highest ON current (Ion) values. Double gate and omega gate type Silicon Nanowire FET has also has lowest OFF current (Ioff) values. OFF current (Ioff) values for Tri gate and Pi gate are also lower but little higher than the other gates. Top gate Silicon Nanowire FET has highest OFF current Values than the rest. For all gate types of Silicon Nanowire FETs, the decrease in Oxide thickness results in a lower OFF Current Values.

V. CONCLUSION

In Summary, we have investigated Current-Voltage (I-V) characteristics of multigate Silicon Nanowire FET. Among all gates, Gate all around has least OFF current values and Top gate has highest OFF current values. Hence, Multigate FET has emerged as best alternate with least leakage current.

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