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Design of 1st Order Switched Capacitor Sigma Delta Modulator for CDMA Using Voltage Divider Biasing of OTA

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***Abstract*--- Wireless terminals with higher capacity and data rates, indicating a new advancement in wireless transceivers. Sigma delta ADC is one of the most used devices in these wireless services. In this work, sample design of 1st order switched capacitor sigma delta modulator is highlighted for CDMA (Code Division Multiple Access). This paper introduces a modified OTA (Operational Transconductance Amplifier) design technique for balancing GBW (unity Gain Bandwidth) and Stability in switched capacitor sigma delta modulators for high frequency applications. For high frequency applications, adjusting the degree of stability with other parameters like as GBW, Slew Rate, and so on is a difficult process. As a result, instead of using separate biasing scheme in the existing method, a voltage divider scheme is used to bias miller series transistors, tail transistors of differential amplifiers, and transistors of output source stage amplifiers all at the same time. In addition, behavioral modelling of a 1st order switched capacitor sigma delta modulator is performed to design OTA for all non-idealities. The effectiveness of the suggested OTA is confirmed by simulation results of a 1st order switched capacitor sigma delta modulator in Cadence Virtuoso utilizing AMS 180nm CMOS technology.**

***Keywords*--- Sigma Delta Modulator, OTA, Stability, Biasing, Transisto**

I. INTRODUCTION

The sigma-delta modulator is the most viable device for meeting multi-mode receiver bandwidth requirements. The use of oversampling and noise shaping by sigma-delta ADCs allows them to provide excellent resolution with low precision components. The oversampling ratio drops as the bandwidth need rises, resulting in a reduction in resolution. It's still difficult to design sigma-delta modulators with good resolution and large bandwidth. As demonstrated in Fig. 1, ADC incorporates analog integrator, comparator as a quantizer, DAC and D flip-flop. Input to the sigma delta ADC is an analog, hence, output is passed through DAC to convert again in an analog before subtract feedback from input. Output of this modulator is digital.[1] Most importantly, the output of modulator is sent back to remove from input signal to the DAC. Next, this result of subtraction is accumulated using switched capacitor integrator where this device acts a low pass filter for signal. At that point, signal is applied to the comparator. Comparator output will be 'one' if integrator is more prominent than zero and output is 'negative one' if integrator is less than zero. At long last, D flip-flop sets the rationale levels of one and zero comparing to one and negative one individually. Among every one of these blocks, integrator dependent on OTA design plays a vital role.[2]

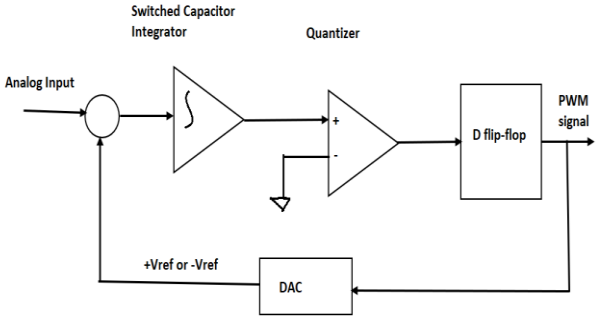

Fig. 1 First Order Sigma Delta ADC

This is very challenging task to adjust stability with other parameter like mainly unity gain bandwidth, slew rate due to miller RHP (Right Hand Plane) zero to use OTA for high frequency applications as shown in Fig.2. In addition to this, gain enhancement is possible by cascading of stages, cascading of stages add poles.[3] Addition of poles means an effort for stability improvement. Further Cascade configuration of OTA also strongly affects the output swing. So, there is restriction on the several stages. The design is expected with efficient stability and gain in order

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to apply in high frequency applications. In this paper, OTA is introduced with modified structure to enhance gain and stability. Output common source stage with source degeneration is used to boost the gain. Stability is achieved with voltage divider biasing scheme [1,2 and 3].[4]

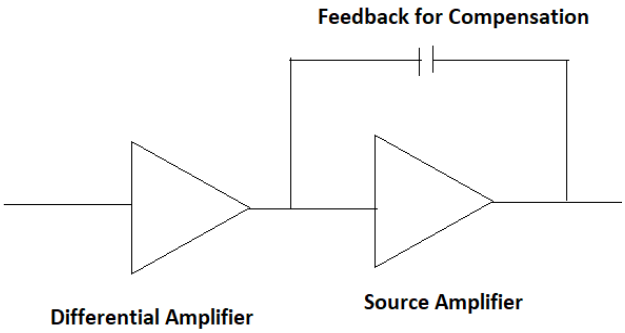

Fig. 2 Basic blocks of CMOS OTA

As shown in Fig. 2, the first stage is a single ended differential amplifier and second stage is source amplifier. Feedback is through miller capacitor to avoid the effect of open loop poles.

II. PROPOSED OTA DESIGN

Proposed OTA circuit is as shown in Fig.4. Relation between SR and GBW is given in equation (1) whereas gain and phase are given in equations (2) and (3). The Optimum value of I10 is designed to increase phase and to keep the minimum power dissipation as given in equation (7). Minimum phase margin (PM)to avoid oscillation in a circuit is 45◦ but at least phase margin of 60◦ is required to improve step response [7]. For phase margin 60◦, Cc is chosen greater than 0.22 times of C_L [9, 10]. The value of C_L should be optimum since maximum value of this load capacitor increases power dissipation and reduces input referred noise [5].

$$\frac{SR}{GBW} = 2\pi \frac{I_B}{gm_1} \quad (1)$$

$$A = gm_1 gm_2 R_1 R_2 \quad (2)$$

$$\tan(\varphi) = \frac{gm_6}{cgs_6} \times \frac{c_c}{gm_1} \quad (3)$$

Design procedure of proposed method is as follows-

$$M_1 = M_2 = \frac{gm1^2}{2*K*I_1} \quad (4)$$

$$M_3 = M_4 = \frac{I_5}{K*(V_{DD}-Vin-Vt-V_{T1})} \quad (5)$$

$$M_6 = \frac{M_3*g_{m6}}{g_{m3}} \quad (6)$$

$$I_{10} = \frac{M10*I6}{M6} \quad (7)$$

$$R_Z = \frac{1}{K*M8*(Vgs8-Vt)} \quad (8)$$

$$V_{gs10} - V_T = V_{gs8} - V_T = \sqrt{\frac{M10}{2*K*I10}} \quad (9)$$

$$R_Z = \frac{1}{M8}\sqrt{\frac{M10}{2*K*I10}} \quad (10)$$

$$Rz = \frac{1}{gm6}\left(\frac{CL+Cc}{Cc}\right) \quad (11)$$

$$M_8 = \left(\frac{Cc}{Cc+CL}\right)\sqrt{\frac{S10}{2*K*I10}}\sqrt{2*K*s6*I6} \quad (12)$$

$$V_{gs8} - V_T \le V_{ds8} \text{ For p MOSFET and} \quad (13)$$

$$M_5 = \frac{2\times I_5}{K_N[V_{ds5}]^2} \text{ and } M_7 = \frac{I_6}{I_5} \times S_5 \quad (14)$$

Where,

$$V_{gs8} - V_T = V_{ds5} \quad (15)$$

Hence effect of non-dominant pole is nullified by adjusting $Z = P_2$, This is achieved by putting equation (8) in equation (9). Then M_8 is designed by equating R_z equations (10) and (11). Aspect ratio of miller series transistor is calculated from M6 and M10. V_{ds5} is designed equal to the Gate to Source voltage of series transistor and accordingly M7 is calculated as shown in equation (14). Along with this, common source stage amplifier with source degeneration is used at output stage as depicted in Fig. 3. This stage increases output resistance of OTA results in increase in gain as shown in equation (16) [4, 8 and 10].

$$A_v = gm_{11}\,(r_{11} + r_6)II\,(r_7) \quad (16)$$

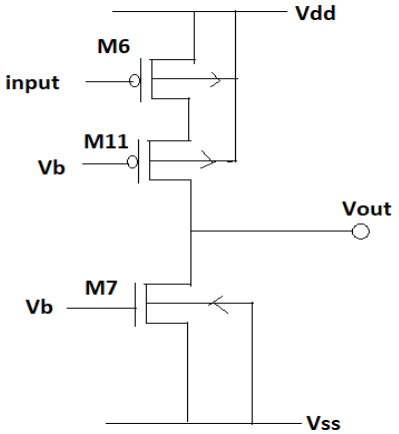

Fig. 3 Common Source Amplifier with Source Degeneration

$$V_{out(max)} = (V_{dd} - V_{ds6} - V_{ds11}) \quad (17)$$

$$V_{ds11} < V_{ds7} \text{ And} \quad (18)$$

$$V_{ds11} < V_{ds5} \quad (19)$$

Further, M11 is calculated as

$$I = \frac{K_p M_{11}}{2}(V_{dd} - V_{ds6} - (V_{gs11} - V_T)) \quad (20)$$

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Slew rate is directly proportional to bias current whereas gain is inversely. Output resistance is increased by reducing aspect ratio of M11 which results in increase in gain.[6]

$$r_o = \frac{1}{\lambda I_d} \quad (21)$$

GBW and stability can be designed properly as per the requirement by adjusting aspect ratio of M10 and M11.

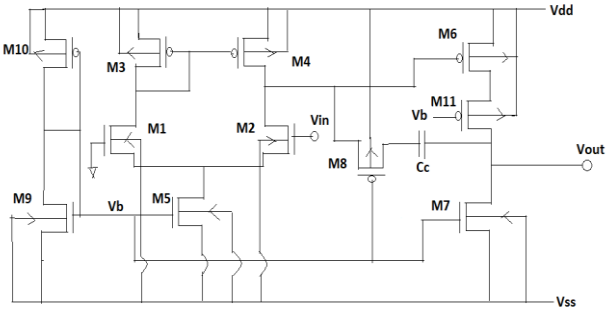

Fig.4 Modified RHP Zero Cancelling Technique

III. SWITCHED CAPACITOR INTEGRATOR

The circuit is depicted in Fig. 5 is obtuse toward parasitic capacitors. As shown in Fig.5, cp2 is constantly associated with Vcm through s4 switch and through connection to inverting input of OPAM. This doesn't change a charge stored on cp2. In like manner, cp1 is charged to Vcm through s2 when s2 closes and this charges to Vin when s1 is closed. In this manner, again there is no change in charge on cp1.This way, design doesn't affect integrating function. Here, c1 and c2 are two non-overlapping clock signals with clock frequency fclk and period T.[7]

Transfer function of switched capacitor integrator is,

$$H(z) = \left(\frac{C_1}{C_f}\right)\frac{Z^{-1}}{1-Z^{-1}} \quad (22)$$

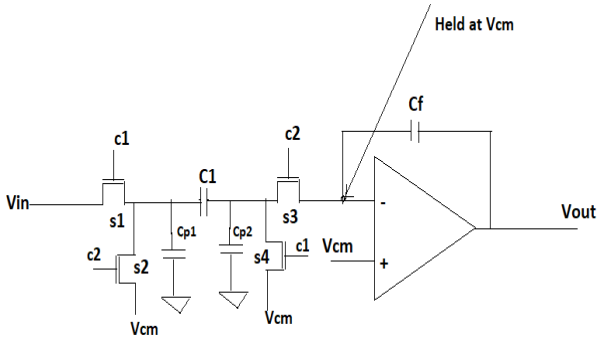

Fig.5 Switched capacitor integrator with parasitic

Design parameters are determined by modeling of non-idealities which affects performance of operational amplifier in the first order switched capacitor sigma delta modulator for this CDMA application as given in Table I [3 and 6].

Table I- Design Parameters

Sr.No.	Parameter	Expected Value
1	Power Supply	±1.8
2	GBW	410MHz
3	CL	0.4 pF
4	SR	407 v/us
5	DC Gain	1000

IV. RESULT

The behavioral simulation of the modulator is tested using the MATLAB Tool. As a result, the OTA parameters are established. Cadence Virtuoso is used to simulate the gate level of a 1st order switched capacitor modulator using the suggested OTA. The inverse relationship between GBW and stability (PM) is seen. The GBW value should be greater than the maximum sampling rate. In order to get a satisfactory step response, the PM should be at least 60°. The comparison of simulation results is shown in the Table II. In comparison, OTA has a GBW of 227MHz and a PM of 73.9°. Miller capacitor with the highest value dissipates power while reducing input referred noise. The proposed OTA dissipates 1.5mW of power. The input and output waveforms of a switched capacitor modulator in CDMA mode with an OSR value of 64 are shown in the Fig. 6. With a 1V input amplitude, the modulator achieves SNDR and SNR values of 36dB and 53dB, respectively. Total power dissipation of 1st order switched capacitor modulator is 18.71mW.

Table II Simulation Results Comparison

Sr.No	Parameter	[3]	[5]	This work
1	Technology(nm)	180	-	180
2	OTA Type	Folded Cascode	Two Stage	Two Stage
2	Gain(dB)	63.7	85	47.9
3	CL(pF)	2	5	0.4
4	Cc(pF)	-	0.5	0.088
5	GBW(MHz)	442	6	227
6	Output Swing(V)	2	2.16	1
7	PM(°)	62	65	73.91
8	Power(mW)	3.78	0.21	1.5

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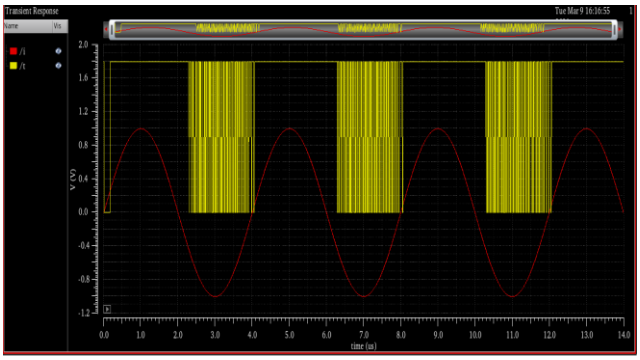

Fig.6 Input and Output of Switched Capacitor Sigma Delta Modulator

V. CONCLUSION AND FUTURE SCOPE

This is seen that stability and gain are inversely proportional to each other. Gain of the conventional structures are good but the stability of suggested OTA is improved. Because the Miller series and source degeneration transistors are properly biased, there is a proper balance between GBW and stability. In conclusion, the Modified RHP zero cancellation method of OTA is suited for use as part of a sigma delta ADC for high frequency applications that demand good gain and stability. The OTA circuit design can be tweaked further to get maximum gain and a good balance of input referred noise and power dissipation.

REFERENCES

[1] M.P. Sarma, N. Kalita, N.E. Mastorakis, "Design of a Low Power Miller Compensated Two Stage OP-AMP Using 45nm Technology For High Data Rate Communication", IEEE 4th international Conference on Signal processing and integrated networks,2017.

[2] T.Nurger,Q.Huang, "A 13.5-mW 185-Msampe/s ΔΣ Modulator for UMTS/GSM Dual-Standard IF Reception", IEEE journal of solid state circuits, vol.36,No.12,Dec.2001.

[3] B.Jose,J.Mathew,P.Mythili, "A Multimode Sigma Delta ADC for GSM/CDMA/WLAN Applications", IEEE Journal of signal processing systems ,vol.62,No. 2,pp.117-130, Feb.2011.

[4] M.M.Ahmadi, "A new Modeling and Optimization of gain-Boosted Cascode Amplifier for High-Speed and Low –Voltage Applications",IEEE transaction on circuits and systems,Vol.53, No.3,Mar.2006.

[5] J. Mahattanakul, J. Chutichatuporn, "Design Procedure for Two Stage CMOS OPAM with Flexible Noise-Power Balancing Scheme",IEEE transaction on Circuits and Systems ,Vol.52,No.8,Aug.2005.

[6] P. Malcovati, S. Brigati, F. Francesconi, F. Maloberti, P. Cusinato and A. Baschirotto, "Behavioral Modeling of Switched- Capacitor Sigma-Delta Modulators", IEEE Transactions on Circuits and Systems-Fundamental theory and Applications, Vol.50, No.3, Mar. 2003.

[7] R.Jacob Baker**,** CMOS Circuit design, layout and simulation**,** third Edition, Wiley Publication,2010.

[8] Marcio Cherem Schneider and Carlos Galup-Montoro, CMOS Analog Design Using All-Region MOSFET modeling**,** Cambridge University press, 2010.

[9] B.Razavi, Design of Analog CMOS Integrated Circuits, Tata McGraw-Hill, Fourteenth Edition, 2008.

[10] P.E.Allen and D.R.Holberg, CMOS Analog Circuit Design , Oxford University Press, 2011