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COMPARISON OF POWER IN CMOS AND ADIABATIC FULL ADDER CIRCUITS USING 0.18µM TECHNOLOGY PARAMETERS

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***Abstract*— This paper presents the design and power comparison of charge-recovering adiabatic full adder circuits and CMOS logic based full adder circuit. The low-voltage Adiabatic Logic circuits have been designed for low-voltage, low-power dissipation and high-frequency operation. A comparative analysis was performed in which logic gates were constructed using adiabatic logic. A layout-based simulation was then performed to verify the operation. Simulation results have shown that the adiabatic logic family is suitable for low voltage operation below 0.18µm CMOS technology. Full adder circuitries are vital mechanisms in applications such as micro processors and microcontrollers. Along with the fundamental addition, full adders are used in performing other useful arithmetic operations such as multiplication, division, subtraction, address calculation, etc.**

In this paper conservative complementary metal oxide semiconductor (CMOS) and adiabatic adder circuits (PFAL, TGAL) are characterized in terms of leakage power, process variations, temperature variations and transistor count using 0.18µm CMOS technology.

***Index Terms*—Adiabatic Switching, CMOS technology, Static power dissipation, Transmission Gates**

I. INTRODUCTION

The main concerns of circuit design are: first, the long operating battery life requirement of electronic devices and the other is because of increasing number of devices on a single chip which leads to reliability and packaging difficulties.

Present electronic devices low-power necessities challenged the researchers towards the study of technological solutions that reduce the energy dissipated by an electronic circuit. The charging and discharging of the node capacitances in the CMOS circuits is the main causes of energy dissipation. Such part of the total power dissipated by a circuit is called dynamic power. Thus an alternative approach of the power dissipation reduction has been proposed, named adiabatic switching in order to reduce the dynamic power. In such approach, the process of charging and discharging of the node capacitances is carried out in such a way that a small amount of energy is wasted and a recovery of the energy stored on the capacitors is achieved. The adiabatic circuits can be classified into two fundamental categories: fully adiabatic circuits and quasi-adiabatic circuits. [1]

In the first class, in particular working conditions, energy consumed in operation is asymptotically zero but their large area and the complexities in design make these circuits not competitive with traditional CMOS circuits where as in second class, circuits designed such that they can recover a large portion of the energy stored in the circuit node capacitances. This tendency however allows a good trade-off between area occupation and circuit complexity.

The circuits implemented here are adder circuits. Since power-efficient multipliers require power efficient implementation of adder circuits to execute complicated algorithms like filtering, FFT in microprocessors and digital signal processors.

II. SWITCHING IN ADIABATIC CIRCUITS

The adiabatic logic gate operation is divided into two distinct stages: one stage is used for logic evaluation; the other stage is used to reset the gate output logic value[1] .In the following section we analyze conventional switching and adiabatic switching in detail.

A. Conventional switching

There are three major sources of power dissipation in digital CMOS circuits namely dynamic, short circuit and leakage power dissipation. The dominant component is dynamic power dissipation and it is due to charging, discharging of load capacitance. The equivalent circuits of CMOS logic for charging and discharging is shown in Fig.1.

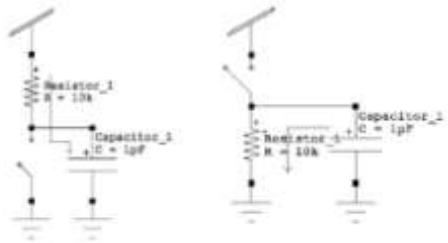

Figure 1. Conventional CMOS (a) Charging (b) Discharging

The expression for total power dissipation is given by

$$P_{tot}=\alpha.C_L V_{VDD}.f_{clk} + I_{sc}V_{VDD} + I_{le}.V_{VDD} \quad (1)$$

here, α is the switching activity, C_L is the loading capacitance, f_{clk} is the clock frequency, V_{VDD} is the supply voltage, I_{sc} is the short circuit current, and I_{le} is the leakage current.[3]

In above equation, the first term represents the dynamic power and second term is due to the direct-path short circuit current I_{sc} which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground.

B. Adiabatic switching

Adiabatic switching can be achieved by ensuring that the potential across the switching devices is kept arbitrarily small. This can be achieved by charging the capacitor from a time-varying voltage source or constant current source as shown in Fig. 2.

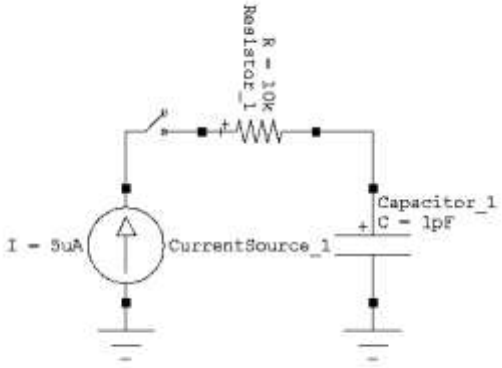

Figure 2. Schematic for adiabatic charging process

$$Vc(t)=Is.t/C \quad (2)$$

Hence the charging current can be expressed as a function of V_C and time t

$$Is=C.Vc(t)/t \quad (3)$$

The amount of energy dissipated in the resistor R from t = 0 to t=T can be found as

$$Ediss = R\int_0^T Is^2\,dt - RIs^2T \quad (4)$$

Combining (3) and (4), the dissipated energy during this charge-up transition can also be expressed as

$$Ediss = \frac{RC}{T}.CVc^2(T) \quad (5)$$

From (5) we can say that the dissipated energy is smaller than for the conventional case if the charging time T >>2RC and can be reduced by increasing the time of charging.

By reversing the current-source direction, a portion of the energy stored in the capacitor can also be reclaimed by allowing the charge to be transferred from the capacitor back into the supply.

Thus adiabatic logic circuits require non-standard power supplies with time-varying voltage, called pulsed power supplies. [3]

C. Cmos inverter

Power dissipation in conventional CMOS circuits primarily occurs during the device switching. When the logic level in the system is "1," there is a sudden flow of current through R.

$Q = C_L.V_{VDD}$ is the charge supplied by the positive power supply rail for charging C_L to the level of V_{VDD}. Hence the energy drawn from the power supply is

$$\mathbf{Q \cdot V_{VDD} = C_L V_{VDD}^2}$$

By assuming that the energy drawn from the power supply is equal to that supplied to load capacitance C_L, the energy stored in C_L is said to be one-half the supplied energy.

$$\mathbf{Estored = (\tfrac{1}{2})C_L\, V_{VDD}^{\,2}.}$$

The remaining energy is dissipated in R. The same amount of energy is dissipated during discharging in the nMOS pull-down network when the logic level in the system is "0." Therefore, the total amount of energy dissipated as heat during charging and discharging is

$$\begin{aligned} Etotal &= Echarge + Edischarge \\ &= 0.5\, C_L\, V_{VDD}^{\,2} + 0.5\, C_L\, V_{VDD}^{\,2} \\ &= C_L\, V_{VDD}^{\,2} \end{aligned}$$

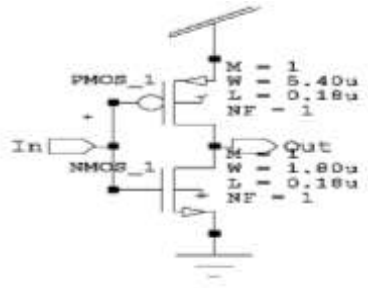

Figure 3. Conventional CMOS Inverter

III. ADDER IMPLEMENTATION

A basic cell in digital computing systems is the 1-bit full adder which has three 1-bit inputs (A, B, and C) and two 1-bit outputs (sum and carry). The relations between the inputs and the outputs are expressed as

$$Sum = ABC + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} \quad (6)$$

$$Carry = AB + BC + CA \quad (7)$$

A. Conventional adder

Conventional CMOS Implementation has two functional blocks pull-up and pull-down. Pull-up functional block is implemented using P-channel MOSFETs and pull down functional block is implemented using N-channel MOSFETs.

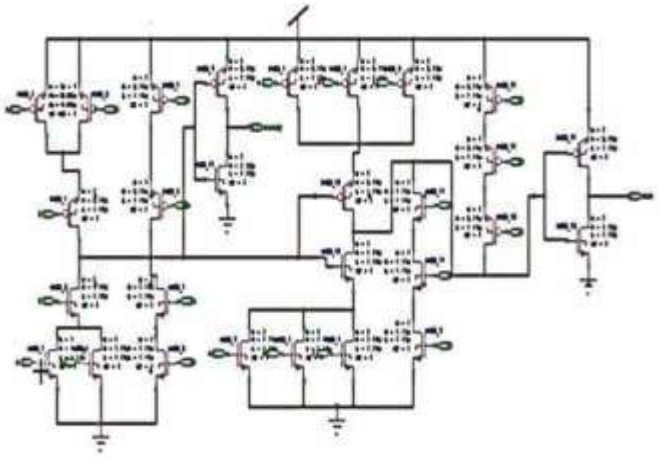

Figure 4: Conventional Cmos Full Adder

B. Transmission gate based adiabatic adder

Functioning of TGAL is like when the control input is a logic zero (negative power supply potential), the gate of the n-channel MOSFET is also at a negative supply voltage potential. The gate terminal of the p-channel MOSFET is caused by the inverter, to the positive supply voltage potential. Regardless of on which switching terminal of the transmission gate (A or B) a voltage is applied (within the permissible range), the gate-source voltage of the n-channel MOSFETs is always negative, and the p-channel MOSFETs is always positive. [2]

Accordingly, neither of the two transistors will conduct and the transmission gate turns off. When the control input is a logic one, so the gate terminal of the n-channel mosfets is located at a positive supply voltage potential. By the inverter, the gate terminal of the p-channel mosfets is now at a negative supply voltage potential. As the substrate terminal of the transistors is not connected to the source terminal, the

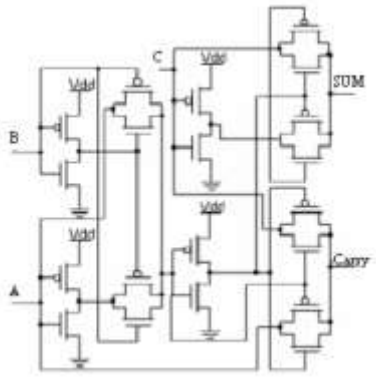

Figure 5. Transmission Gate Based Adiabatic Full Adder

C. Positive feedback adiabatic logic (pfal) adder

The pfal gate has two cross coupled inverters and two functional blocks f and /f driven by normal and complemented inputs which gives both normal and complemented outputs. Both the functional blocks have been implemented with n channel mos transistors. [2]

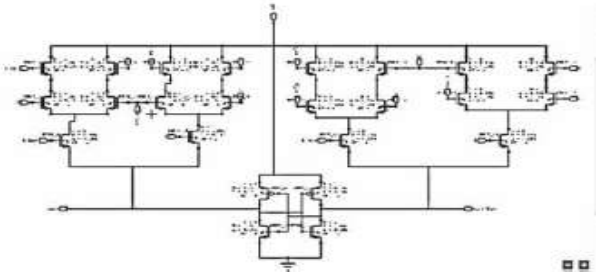

Figure 6 (a). PFAL Based Adiabatic Full Adder for SUM

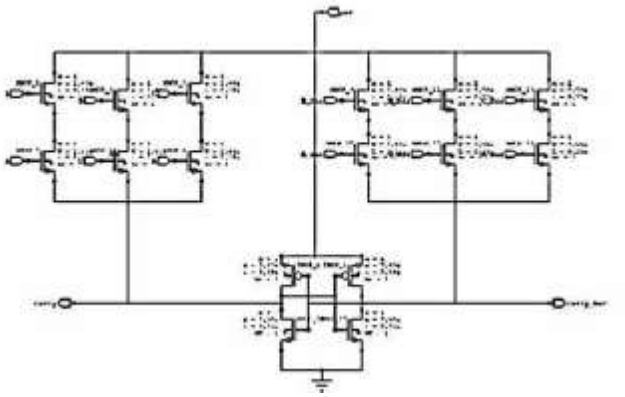

Figure 6 (b). PFAL Based Adiabatic Full Adder for CARRY

IV. SIMULATION RESULTS

The simulation is done at 180nm technology for comparison of power dissipation. The circuits are designed in tanner eda tool and simulated at normal room temperature. The maximum supply voltage used is 1.8v.

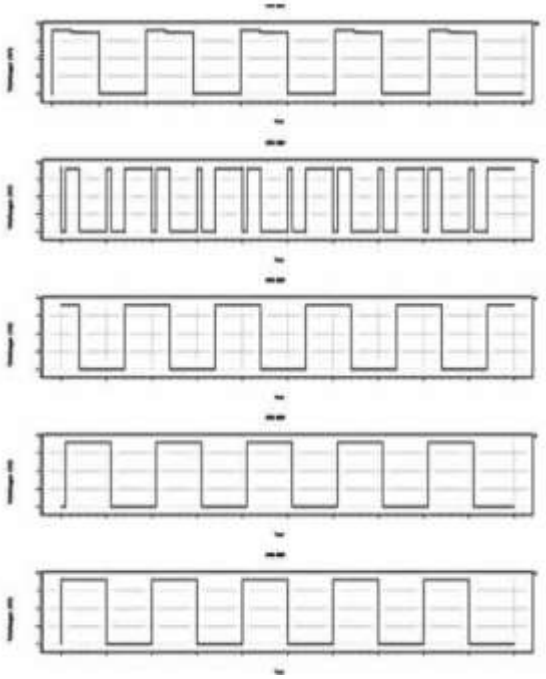

Figure 7: Transient Analysis Results For Cmos Full Adder

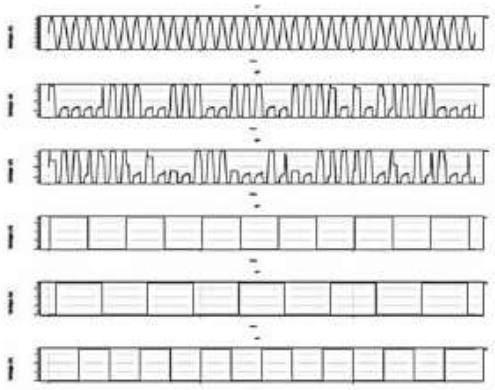

Figure 8: Transient Analysis Results For Tgal

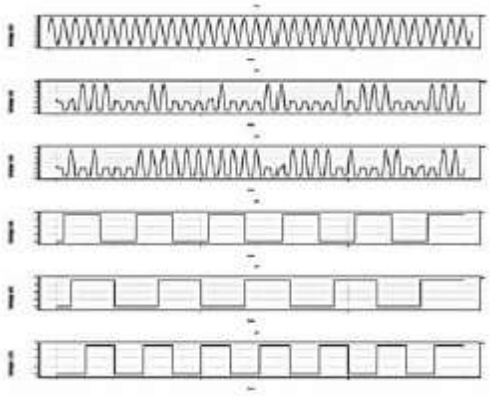

Figure 9: Transient Analysis Results For Pfal

V. COMPARATIVE ANALYSIS

Following are the characterization graphs for various adder circuitry for power dissipation across process variations (viz. Typical nmos –typical pmos tt, slow nmos - fast pmos sf, fast nmos -slow pmos fs, fast nmos –fast pmos ff and slow nmos -slow pmos ss) ; temperature variations (viz. 0 °c, 25 °c and 80°c) and power supply variations of ± 10%.

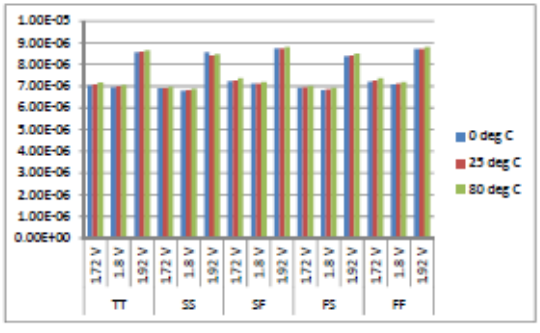

Figure10: Power Dissipation Results For Cmos Adder

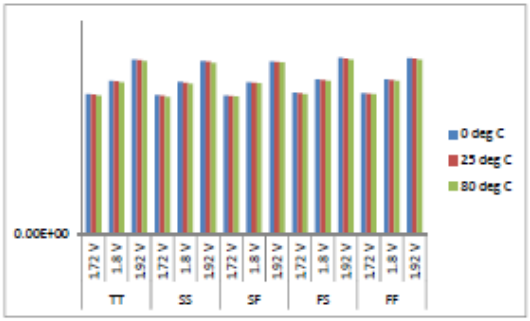

Figure 11: Power Dissipation Results For Tgal

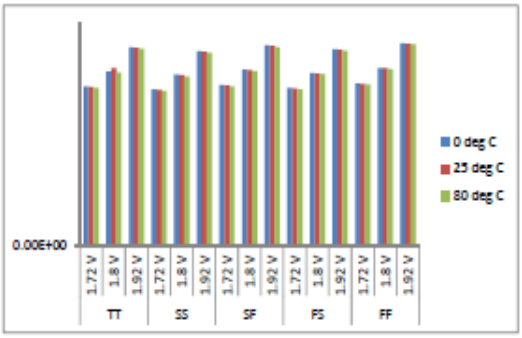

Figure 12: Power Dissipation Results For Pfal

TABLE 1: RESULT COMPARISON FOR VARIOUS ADDERS IN 180NM CMOS TECHNOLOGY.

Parameter	Adder Type		
	CMOS	PFAL	TGAL
Transistor count	28	10	38
Power Diss.(W)	0.00000694684	1.091233E-33	5.029481E-33

TABLE 2: RESULT COMPARISON FOR VARIOUS PROCESS VARIATIONS IN 180NM CMOS TECHNOLOGY.

Parameters	Best Case Results				Worst Case Results			
	Tech.	O/P Value	Process	Volt. (V)	Tech.	O/P Value	Process	Volt. (V)
Power Dissipation	PFAL	9.69E-34	Slow Slow ,80 deg C	1.72	CMOS	8.815 E-06	Slow Fast, 80 deg C	1.9

VI. CONCLUSION

This paper deals with the performance comparison of various adiabatic adder circuits with traditional CMOS adder circuit. The analysis and simulation results shows that the circuit designs based on adiabatic standard gives better-quality performance when compared to established approaches in terms of power even though their transistor count is high in some circuits. Hence for ultra low power requirements adiabatic logic is an efficient alternative for customary CMOS logic circuit design.

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