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Performance Investigation of Multilevel Inverter Based Static Synchronous Series Compensator for Power Flow Control

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Abstract: **-- This paper consists of control logic of Five-Level Flying Capacitor Multilevel Inverter (FCMLI) based Static Synchronous Series Compensator (SSSC) has been proposed. SSSC which is connected in series with the transmission line is preferred to other compensating devices because apart from controlling the active and reactive power flow, it helps to damp out unnecessary oscillations, reducing the Sub-Synchronous Resonance (SSR) and helps in improving the Power Quality (PQ). Hence, FCMLI is used which helps to ameliorate the output waveform and reduces the auxiliary filtering requirements. Moreover, the control logic for the inverter that has been shown in such a way that voltage stress across each capacitor connected to DC-link voltage is equal. The control logic has been implemented in MATLAB/Simulink environment and the result is shown as there are no SSR phenomena and considerable less line loss.**

Index Terms: **— Multilevel Inverter, FCMLI, Power Oscillation, Power Quality, FACTS-Controller, SSSC, SSR, VSC, SPWM**

I. INTRODUCTION

In today's world, there has been always an ever growing demand in electricity because of rapid growth in industrialization and increased standards of living of the people. As electricity consumption is increasing, so proper quality of power and its reliability is highly desired. For that the concept of a Flexible AC Transmission System (FACTS) comes into picture. The use of high-power electronics equipment under the concept of FACTS is a must that increases the transmission capacity, controls power flow in the transmission line and enhances the performance of the existing systems. Apart from these, it also helps in mitigating the PQ issues in present deregulated and highly competitive power industry. Basic FACTS controllers are the Static Compensator (STATCOM), the Static Var Compensator (SVC), the Unified Power Flow Controller (UPFC), the Interline Power Flow Controller (IPFC) and the Static Synchronous Series Compensator (SSSC). Therefore, the inverters should be such that its power handling capacity should be high, performance is good and is relatively inexpensive for the achievement of FACTS. But in near future it may so happen that the utilization of these inverters will be problematic because the power-electronic devices have their functional limitations. For high power applications voltage range is also large (more than 2KV) and the semiconductor devices require just a fraction of it. Hence, series connected FACTS devices is preferred that is capable of handling such voltage range [2].

Among series connected FACTS devices, SSSC consists of a converter which is connected in series to a transmission line through a coupling transformer. The SSSC using voltage source inverters has tremendous merits for transmitting power over a long distance such as:

1) Improves power system stability,
2) Increases the transmission lines capacity
3) Controls the power flow,
4) Damp out power system oscillations and Sub-Synchronous Resonance (SSR) [8]. Since, both voltage and power requirement are high, design of multilevel inverter (MLI) for SSSC should be well suited. In general Multilevel Inverter classifications are

i) Diode-Clamped Multilevel Inverter (DCMLI)
ii) cascaded H-bridge inverter
iii) Flying Capacitor based multilevel inverter (FCMLI).

The demerit of DCMLI is that it is subjected to voltage imbalance in the DC-link. Similarly, in H-bridge inverter in order to lessen the harmonics enormous number of inverters is required and the voltage regulation loop is quite difficult. In addition to that, as power undulates two times of the frequency for the interchange of reactive power, this leads to requirement of over-sized link capacitors. So, as far as such above-mentioned limitations are considered FCMLI is considered to be the best alternative. FCMLI along with capacitors connected in a cascaded manner aids in declining the difficulties especially during the transient conditions. Further, the control strategy in FCMLI is very simple to implement as that of a normal two-level inverter and does not depend on the voltage level across the output. This is

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possible as the voltage gets balanced is distributed among several switches of lower ratings. As a result, the voltage stress across the devices is equal. With redundancy in the switching combination, this structure makes it possible to attain enhancement in the output voltage waveform. As the desired value is almost achieved so, there is no requirement of unnecessary expenditure on filtering the output [4]. In this paper we propose the design of control logic of a five-level FCMLI-based SSSC. Principle of SSSC and its distinguished features have been explained in Section II. Further basic configuration of Flying Capacitor based MLI, its Switching Scheme, Modulation Strategy, Control Logic in MATLAB/Simulink is presented in Section III. The Simulation results of proposed Control Logic have been discussed in Section IV and the conclusion has been presented in Section V.

II. SSSC

The Static Synchronous Series Compensator (SSSC) is one of the FACTS controller devices which are connected cascaded to the line. It is a semi-conductor based voltage source inverter, where the input is sinusoidal in nature of varying magnitude whose block diagram is represented in Fig. 1. It consists of a) Voltage Source Converter (VSC) where the control technique is applied b) Transformer that links the SSSC to the main line c) Energy Source (which is optional) which contributes to the DC capacitor voltage, and neutralize the losses in the system [9]. Distinguished features of SSSC over other series compensating devices are its constant compensating voltage which is independent of line current, provides fast control and is inherently neutral to SSR [1],[3],[6].

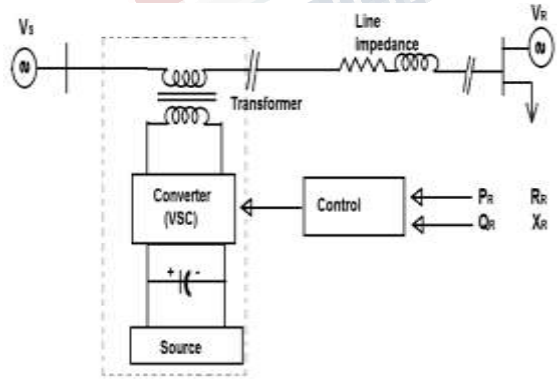

Fig.1. Block diagram of SSSC connected to line

The operation of SSSC either with or without an external electric power source acts as a series compensating device whose output voltage is independently controllable of the line current. Its objective is to increase or decrease the total reactive voltage drop across the line and thereby the transmitted active power is controlled [8]. There are generally three modes of operation of SSSC and they are Normal Mode of Operation, Inductive Mode of Operation and Capacitive Mode of Operation [9]. SSSC employed in elementary two machine system and phasor diagram for capacitive mode of operation is given in Fig.2. Here, *V1*: Sending end voltage *V2*: Receiving end voltage α: Difference in phase between the two end voltages. *I*: Current flowing from *V1* to *V2* *VL*: Line impedance voltage drop *PQ*: Active power *VQ*: Voltage impressed by SSSC The injected voltage is almost about 90˚ to the line current. But a fraction of the incoming voltage is in same phase with the line current that leads to notable drop in the inverter. But the remaining part of the impressed voltage which is 90˚ with the line current, imitates inductive or capacitive reactance in series with the transmission line. This emulated changing reactance, introduced by the incoming voltage source, accelerates the electrical power flow through the transmission line [8].

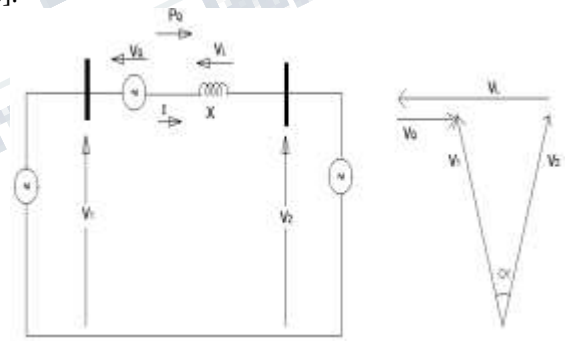

Fig.2.The conventional two-machine system employing SSSC and related phasor diagram

The governing equation expressed for a two machine system is given by:

$$P_Q = \frac{V^2 \mathrm{Sin}\alpha}{X} + \frac{V}{X} V_Q \mathrm{Cos}\frac{\alpha}{2}$$

The transmitted power due to SSSC either improves or declines by a fixed proportion of the peak

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power which is exchangeable by an un-compensated line. It is independent of α□ □ that lies in the range of*0* □ □*α*□ □ □*90*□ . Further, if this incoming voltage is greater than the voltage considered across the un-compensated line between both the ends, then the power flow will be opposite in direction [4], [8]. Q Q 2VSinα V α P = + V Cos X X 2

III. FLYING CAPACITOR BASED MLI

A. Basic Configuration

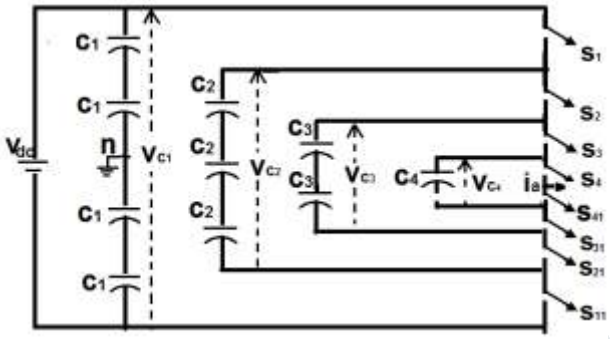

Fig.3. Arrangement of capacitors in one phase FCMLI

Fig.3. shows the arrangement of capacitors in a five-level flying capacitor inverter for one phase only. In the figure there are 8 switches and they are S1, S2, S3, S4, S11, S22, S33, S44 and along with it anti-parallel diodes are connected. The switching of pair of switches occurs in a reciprocal fashion. Considering a case, if S1 is ON, then S11 is OFF and contrariwise. Voltage across each capacitor is identical. Considering capacitor of the first leg near to among which C1, being the main DC link Capacitor is required to be controlled external to the system. So, an accumulator of suitable rating is connected as the external source. The number of capacitors in each leg goes on decreasing by 1 starting from the main leg to the innermost leg. Total number of capacitors, main DC bus capacitors, voltage of the innermost capacitor is presented in Table I. dc ○

Table I Number of Capacitors and Voltage per phase in FCMLI

Clamping capacitor per phase	$\frac{(n-1)^2}{2}$
Main DC-link bus capacitors	$n-1$
Voltage across the innermost capacitor	$\frac{V_{dc}}{n-1}$
Voltage across the next innermost capacitor	$\frac{V_{dc}}{2(n-1)}$

Similarly, it follows for the other two phases with the same construction which are coupled to the same dc-link. C1 is the main DC-link capacitor and apart from that, the three capacitors are the flying-based capacitors which actually help in providing the desired voltage range. The flying capacitors of every phase are independent [4].

B. Switching Scheme

Table II Switching scheme of 1-phase leg of 5-level FCMLI

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S_1	S_2	S_3	S_4	C_2	C_3	C_4	V_{an}
1	1	1	1	UC	UC	UC	$V_{dc}/_2$
1	1	1	0	UC	UC	+	$V_{dc}/_4$
1	1	0	1	UC	+	−	$V_{dc}/_4$
1	0	1	1	+	−	UC	$V_{dc}/_4$
0	1	1	1	−	UC	UC	$V_{dc}/_4$
0	0	1	1	UC	−	UC	0
0	1	0	1	−	+	−	0
0	1	1	0	−	UC	+	0
1	0	0	1	+	UC	−	0
1	0	1	0	+	−	+	0
1	1	0	0	UC	+	UC	0
1	0	0	0	+	UC	UC	$-V_{dc}/_4$
0	1	0	0	−	+	UC	$-V_{dc}/_4$
0	0	1	0	UC	−	+	$-V_{dc}/_4$
0	0	0	1	UC	UC	−	$-V_{dc}/_4$
0	0	0	0	UC	UC	UC	$-V_{dc}/_2$

The switching combination of the four switches along with three flying capacitor to get a desired waveform is such that a) If all the switches are ON/OFF and the capacitor value remains UC (unchanged), then output voltage is either or . Similarly, if any three switches are ON/OFF, then output voltage is either or . If any two switches are ON irrespective of the capacitor value, then output voltage is 0. It can be seen that as there is a constant repetition of output voltage, this calls for better choice of switching so that desirable output is achieved. Here, the switching pair is optimized in such a way that they do not adversely affect the capacitor. Moreover, it minimizes the capacitor cost and losses in the system. dc +V /2 dc -V /2 dc +V /4 dc -V /4

C. Modulation Strategy

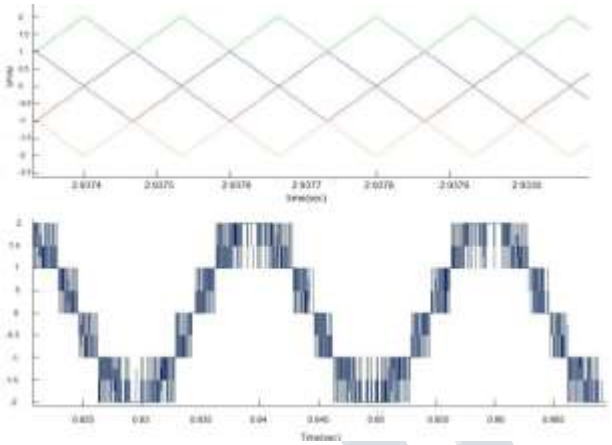

Fig.5. Modulation Strategy a) SPWM b) Output Waveform

The modulation strategy for the inverter considered here as shown in Fig.5 is based on sinusoidal pulse width modulation (SPWM). This scheme is preferred for the suppression of harmonics and reduction in switching losses. Here, the carrier signal in triangular form is compared to a sinusoidal signal and the corresponding output of modulated signal is presented in Fig.5 (b). Here, for a five-level MLI, a modulating sinusoidal signal and four carrier triangular waves are compared for all the three phases of the inverter. Accordingly, output waveform appears in stages. Though, the magnitude of modulating signal of three-phase are equal, they are phase shifted by some angle. The logic applied is such that when the modulating signal exceeds the carrier wave the output of the comparator is positive unity otherwise zero. The outputs of these comparators are arithmetically combined to generate output voltage at the different stages.

D. Five-Level FCMLI & Control Logic

A Five-Level Flying Capacitor MLI based on SSSC is used for control of both active and reactive power and keeps the entire power system under stability limits as shown in Fig.6. It is connected in cascaded manner to the main line and the voltage injected is such that its magnitude and phase are both manageable. Again this incoming voltage is almost in 90˚ to the current flowing in the line and hence, controls the power flow. A five-level FCMLI is simulated using MATLAB/Simulink environment with the system parameters as given in Table III.

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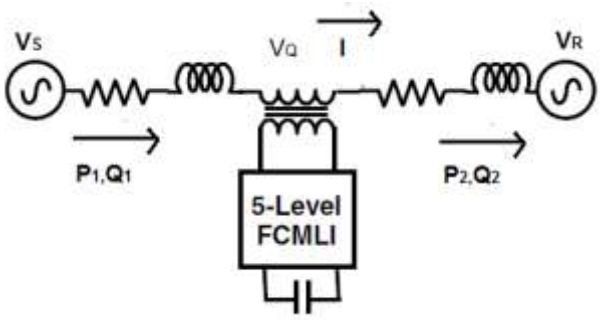

Fig.6. FCMLI connected to transmission line.

Table III Specification for the design of FCMLI

Voltage Magnitude (L – L,rms)	154 KV
Frequency	50 Hz
Angle Difference between Sources	30°
Capacitance	2200μF

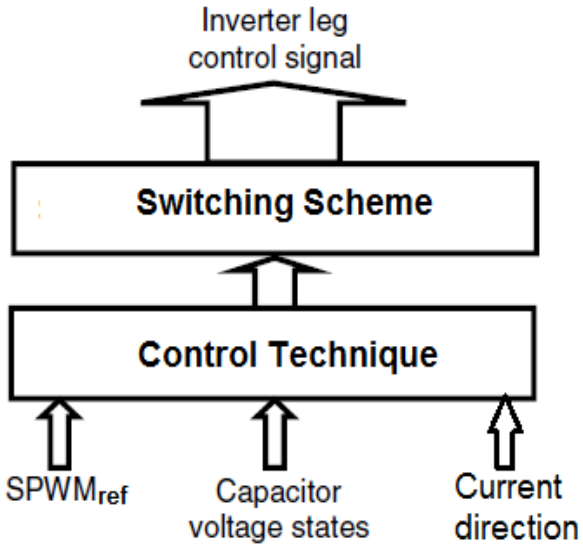

Fig.7. Block diagram of Control Algorithm

The block diagram of control algorithm in Fig.7 involves the technique of managing the voltages of flying capacitor around its reference dc-voltage values along with producing the desired level of voltage at the output. In this case, dc bus voltage Vdc which is taken under consideration needs an external adjustment. The SPWM modulation scheme discussed already represents the range of voltage that should be produced at a particular point of time. In addition to that, the control technique requires the additional data regarding the current orientation of the inverter and voltage status of the capacitor, which are obtained from suitable devices and networks. As per the control logic given in Fig.8 (reference Power) and (actual Power) obtained from and generates an error which is fed to PI Controller-I. Again further the signal is subtracted from and fed to PI Controller –II. Its output angle β is then added to θ, and then SPWM signal is generated on comparing sinusoidal signal with triangular signal. Then the Switching Strategy is obtained which controls the 5-level FCMLI. Pref actual P ref V ref I d,actual ○

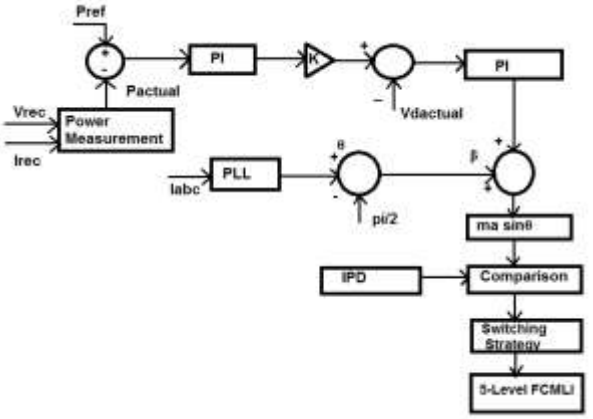

Fig.8. Control Logic of 5-level FCMLI

IV. RESULTS

For the analysis of the functioning of the proposed SSSC based Flying Capacitor based MLI, simulations in MATLAB have been done. The results obtained are shown as follows.

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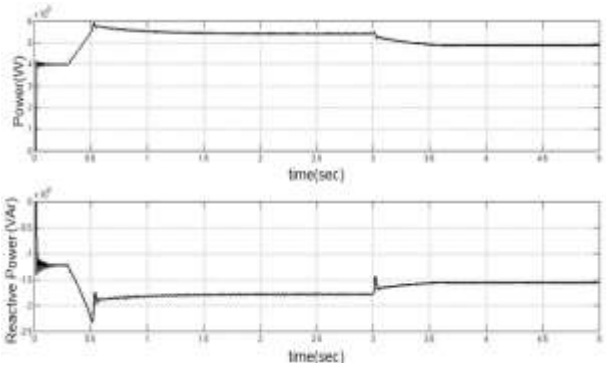

Fig.9. Variable DC Voltage strategy

Fig.9. represents the simulation result of Variable DC voltage strategy. Initially from 0.5 sec to 3 sec, was 5.4 MW and after 3 sec it changed to 4.8 MW. Simultaneously the reactive power also changed [5]. Fig.10. shows that there is no SSR phenomenon as the compensating voltage is 90˚ to line current which is the inherent property of SSSC and helps in improving the power quality. ref P

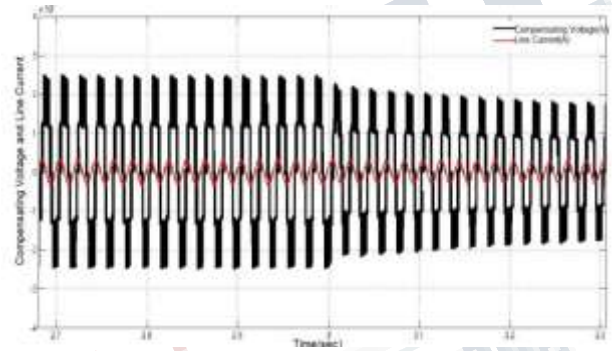

Fig.10.Simulation result for Compensating Voltage and Line Current

Fig.11. shows the simulation result of the inverter output voltage and inverter output current. The inverter output voltage changes at 3sec based on the changes shown in Fig.9 and remains between 10 KV and -10 KV. At the same time the inverter output current remains between 6KA and -6KA after 6sec.

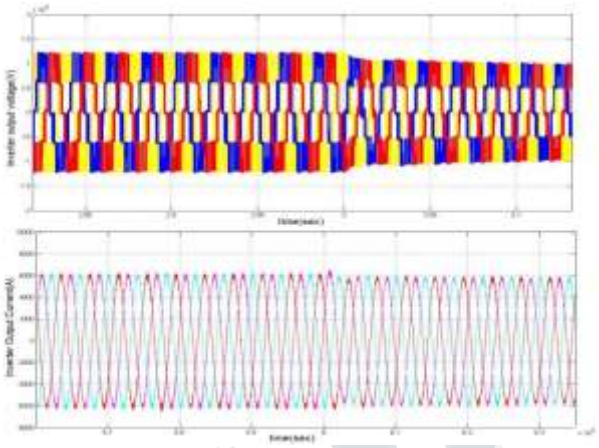

Fig.11. Simulation result of a) inverter output Voltage b) inverter output current

Fig.12. shows the simulation result of capacitor voltage and DC link. Here, the reference DC Voltage is taken as 30KV and it is observed that based on the reference voltage the individual capacitor voltage got balanced at starting from to . The same phenomenon is represented in Fig.13, where the capacitor voltage balancing occurs even if the reference voltage changes after 3 sec [7]. 1 CV 3 CV

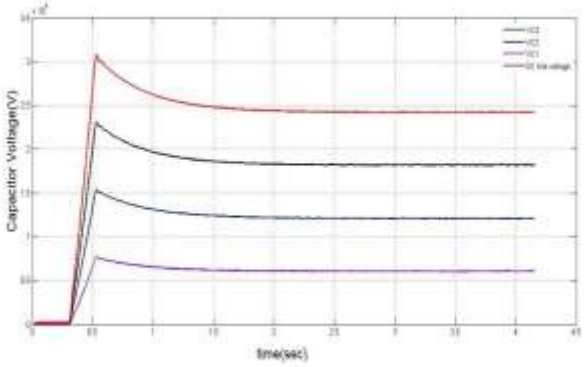

Fig.12. Simulation result of individual Capacitor Voltage

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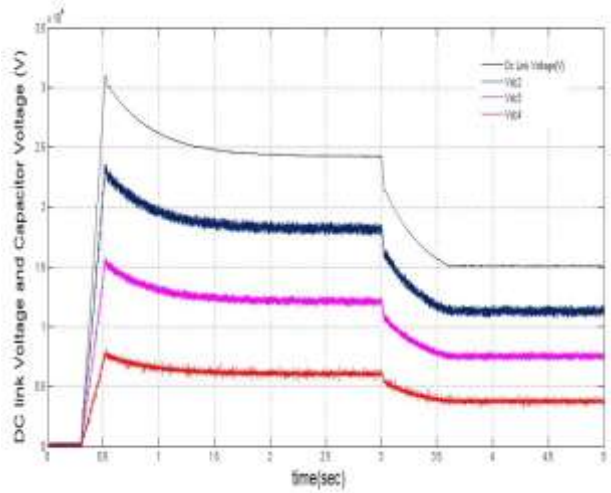

Fig.13. Simulation result of DC link voltage and capacitor voltage

V. CONCLUSION

Hence, the simulation results of control logic developed for FCMLI based SSSC were verified. There is less voltage stress cross the individual capacitor as the voltage gets balanced. Better performance is obtained in terms of SSR, power oscillations and smoothness of output voltage profile.

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