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A Switched Capacitor based Multilevel Inverter using Stepped Waveform Technique

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Abstract: **It is pretty preferable to adapt high frequency (HF) transmission rather than low frequency AC power distribution systems (PDS).Because HF inverter acts as source side in HFAC PDS. A new switched capacitor (SC) based multilevel inverter (MLI) is proposed in this paper which is designed by SC at frontend and H-Bridge backend. SC is connected in series and in parallel to increase the number of voltage levels. With increase in number of voltage levels total harmonic distortion (THD) can be reduced. A stepped waveform method is proposed in this paper to determine the switching angles. The circuit topology, stepped waveform technique, operation, Fourier analysis, parameter determination and topology enhancement are examined. An experimental prototype with output frequency of 25 kHz is implemented to compare the results.**

Keywords:**—Cascaded H-Bridge, high frequency (HFAC), multilevel inverter, switched capacitor, stepped waveform technique**

I. INTRODUCTION

High frequency PDS are more economical than low frequency PDS due to lesser components and more economical. The existing system can be found in renewable energy microgrid systems [1], telecom [2], and electric vehicle [3]. Also HFAC PDS has its limitations towards high power capability, High electromagnetic interference and huge power loss [4]. A HFAC PDS is made up of HF inverters, an HF transmission network, huge number of voltage regulation modules. The most adapted method for higher power transfer capability is to connect the HF inverters in series or in parallel. Due to HF dynamics, it is impractical to synchronise both amplitude and phase by an HF inverter. MLI is a potential solution to increase power capability without synchronisation consideration and lower switch stress. Multilevel inverter significantly simplifies filter design due to the fact that higher number of voltage levels reduces the THD of a staircase output [5]. These HF distribution systems can be in electrical vehicle due to the moderate size of distribution network and effective weight reduction [6]. The operating frequency consideration has to compromise between ac inductance and resistance [7]. So MLI with output frequency of 20 kHz is feasible for EV application.

The traditional topologies of multilevel inverters are diode-clamped and flying capacitor type [8], [9]. The diode-clamped MLI uses diodes to clamp the voltage level, and the flying capacitor MLI uses additional capacitor to clamp the voltage.

As number of voltage levels increases the complexity in these two topologies will increase. A cascaded H-Bridge is another sort of MLI formed by series connection of H-Bridges [10], [11]. The basic circuit is familiar to traditional DC-DC converter [12]. The cascaded model increases the system reliability because of same circuit cell, control structure and modulation. But the disadvantages of cascaded H-Bridge MLI are more switches and number of DC sources. In order to increase two voltage levels in stair case output, an H-Bridge is constructed by four switches and individual inputs are needed. A cascaded H-Bridge can obtain any number of voltage levels, but it is inappropriate to the application of cost saving and input limitation.

After numerous studies a SC based MLI can be implemented to increase the number of voltage levels efficiently. However, control strategy is complex and electromagnetic interference becomes more devastating due to discontinuous input currents [13]. A single phase five level pulse width modulation (PWM) inverter is constituted by a full bridge of diodes, two capacitors and a switch. However, it provides output with only five voltage levels, and higher number of voltage levels are limited by circuit structure [14]. A SC based circuit was presented. However, both complicated control and increased components limit its applications [15]. Further studies were made for the conversion of SC into series and parallel connections. However, it is not apt for the high frequency applications because of multicarrier MPWM [16, 17].This tem the carrier frequency tends to reach a couple of mega Hz for the output frequency to be 20 kHz. For the sake of HF output, high switching losses are inevitable, because the carrier frequency would reach dozen times the output frequency. A SC based MLI can increase the voltage levels when it is used in

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combination with the H-bridge. This is done by connecting the SC in series or in parallel whenever it is required. It is not convenient to use SC because of its control. So it would be a challenging task to present MLI based on SC with HF output, low output harmonics and high conversion efficiency [18].

So based on studies mentioned above a new MLI and simple modulation strategies are presented to act as HF source. The rest paper organised as follows. The discussion of twenty-five level inverter is presented in section-II, including circuit topology, modulation strategy, operation cycles and Fourier analysis. The parameter determination and loss analysis are discussed in section-III. The performance evaluat ion is accomplished by simulation in section-IV followed by concluding remarks.

II. SC BASED CASCADED MLI WITH 25 LEVEL OUTPUT.

The proposed circuit topology is made up of SC frontend and cascaded H-bridge backend. If N1 and N2 are the number of levels obtained by SC frontend and H-bridge backend respectively, then the number of voltage levels is [2×[N1 +N2]]+1 on entire operation cycle.

A.Circuit topology

Fig.2 shows the circuit topology of twenty-five level inverter (N1=6, N2=6), where s1, s2, s3, s4, s5, s6, s_1^ ı, s_2^ ı, s_3^ ı, s_4^ ı, s_5^ ı, s_6^ ıas switching devices of SC circuits (sc1, sc2, sc3, sc4, sc5, sc6)parallel connection of c1,c2,c3,c4,c5,c6. s1a, s1b, s1c, s1d, s2a, s2b, s2c, s2d, s3a, s3b, s3c, s3d, s4a, s4b, s4c, s4d, s5a, s5b, s5c, s5d, s6a, s6b, s6c, s6d are the switching devices of cascaded H-bridge. vdc1, vdc2, vdc3, vdc4, vdc5, vdc6 are the input voltages. D1, D2, D3, D4, D5, D6 are the diodes to restrict current direction. Iout and v0 are the output current and voltage respectively.

It is worth noting that backend circuit of the proposed inverter is cascaded H-Bridges in series connection. It is significant for H-Bridge to ensure the circuit conducting regardless of direction of current and output voltage. In other words, circuit has four conducting modes in the conditions of resistive and inductive loads, i.e. , forward conducting, reverse conducting, forward freewheeling and reverse freewheeling.

B. Stepped Waveform technique

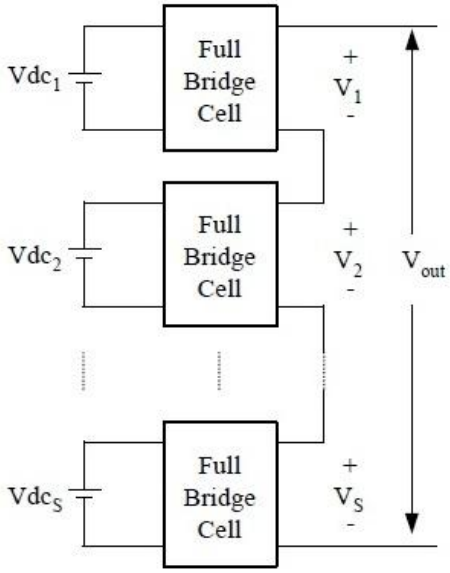

Fig.1. Schematic diagram of s H-Bridge series connected multilevel inverter.

There are many modulation methods to regulate the multilevel inverter. In this paper stepped waveform technique [19] is used. As shown in Fig.1, S H-Bridge cells are connected in series. An output voltage of waveform can be obtained by summation of output voltage of each cell, i.e.

$$Vout=V1+V2+V3+\ldots\ldots +Vs \quad (1)$$

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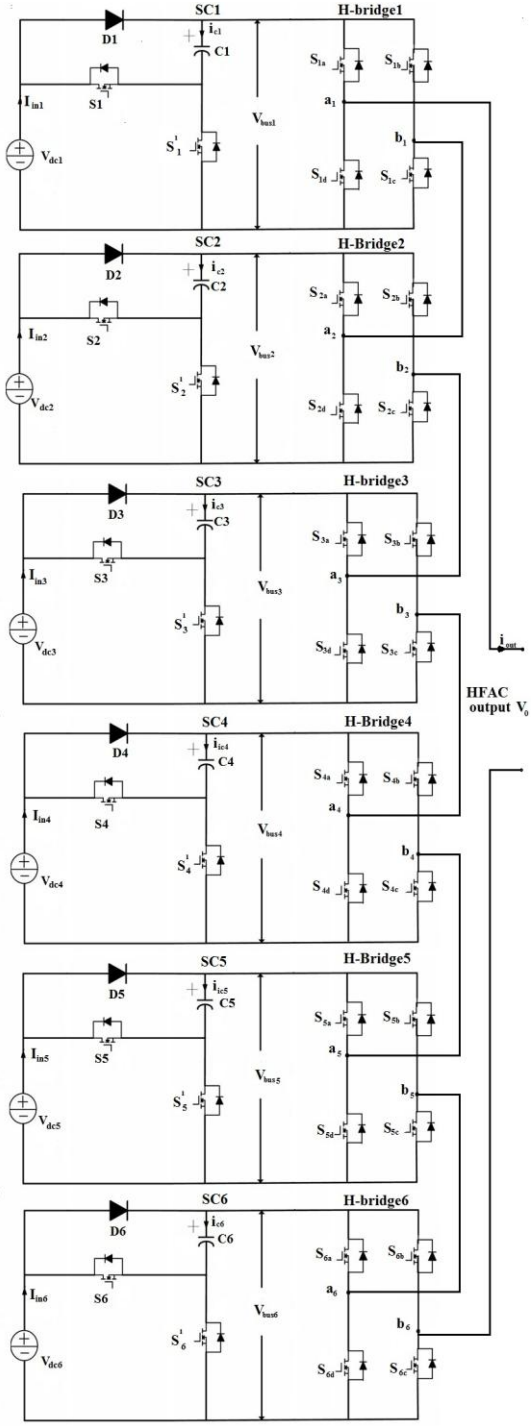

Fig.2. Circuit topology of cascaded twenty-fivelevel inverter(N1=6, N=6)

Fig.1 illustrates a generalised waveform of S H-Bridge inverters in series connection. As we know that, [2[N1 +N2]] +1output levels can be obtained with S H-Bridges, capacitors and dc sources.

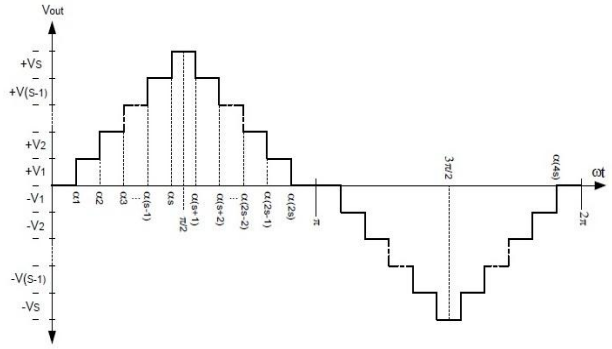

Fig.3 Output voltage of the MLI with s number of levels.

From the voltage waveform in Fig.3 it consist of 4s switching angles, α1, α2, α3 ... α(4s-1), and α4s, in each cycle. The voltage of the first level equals V1; the voltage of the second level equals to V2 and so on. These voltage amplitudes supplied by dc sources are equal in this paper. Here, in this paper the step spaces and the height of voltage levels are equal.

In general, the modulation index of sinusoidal pulse width modulation (SPWM) is the ratio of modulating signal amplitude to the carrier signal amplitude. For the specified multilevel case, the modulation index is as follows:

$$M = \frac{V_{out}}{S \times V_{dc}}$$

Where

Vout is the amplitude of output voltage at the fundamental frequency.

S is the number of dc sources.

Vdc is the amplitude of dc sources.

C .Quarter-Wave Symmetric Multilevel Waveform

The stepped waveform is assumed to be the quarter-wave symmetric. The relationship among the switching angles of the waveform shown in Fig.3 can be found as follows:

In the second quarter;

$\alpha_{s+1} = \pi - \alpha_s$, ..., $\alpha_{2s-1} = \pi - \alpha_2$, $\alpha_{2s} = \pi - \alpha_1$. (2)

In the third quarter;

$\alpha_{2s+1} = \pi + \alpha_1$, ..., $\alpha_{3s-1} = \pi + \alpha_{s-1}$, $\alpha_{3s} = \pi + \alpha_s$. (3)

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In the fourth quarter;
$\alpha_{3s+1}= 2\pi-\alpha_s$, ..., $\alpha_{4s-1}=2\pi-\alpha_2$, $\alpha_{4s}=2\pi-\alpha_1$. (4)

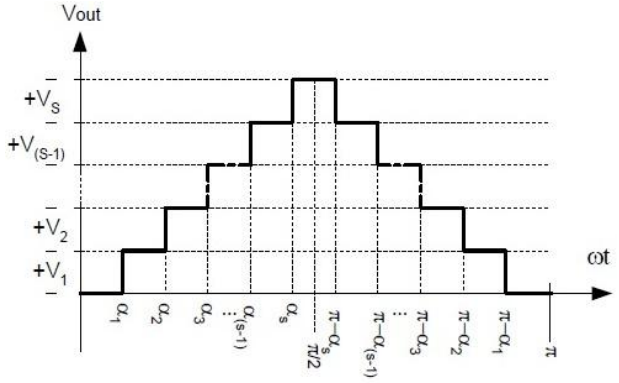

Fig.4 Half cycle of multilevel inverter waveform

The first half cycle of the proposed quarter-wave symmetric waveform is depicted in Fig.4. The output voltage level is zero from ωt = 0 to ωt =α_1 . At ωt =α_1, the output voltage level is changed from zero to +V1, and from + (V1+V2) at ωt =α_2. This processes will be repeated until ωt = π/2, and the output level becomes +V1+V2+.....+V(s-1)+Vs. Then in the second quarter, the level of output voltage will be decreased to +V1+V2+.....+V(s-1) at ωt =π-α_s. The process will be repeated until ωt =α_1 and voltage becomes zero again. In the second half of the waveform, the processes will be repeated all of the previous steps except the amplitude of the dc sources change from positive to negative. The next period will then repeat the same cycle.

D. Fourier series of the proposed waveform.

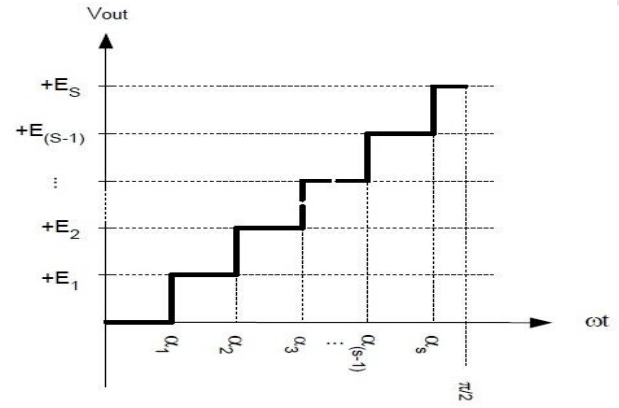

Fig.5 First quarter of the quarter-wave symmetric waveform

Because of quarter-wave symmetric characteristic, which is illustrated in Fig.5, the Fourier series coefficient is given by

$$a_n=\frac{4}{\pi}\int_0^{\frac{\pi}{2}} f(\omega t)\sin(n\omega t)\,d(\omega t)\ ,\ \text{for odd n} \qquad (5)$$

$a_n = 0$, for even n (6)

And

$b_n= 0$, for all n (7)

Where

$f(\omega t)=V_{out}(\omega t)$ (8)

For all n, from equations (5) to (8), the Fourier series given as

$$f(\omega t)= \sum_{n=1}^{\infty} a_n \sin(n\omega t) \qquad (9)$$

From equation (5), let α= ωt Hence

$$a_n=\frac{4}{\pi}\int_0^{\frac{\pi}{2}} f(\alpha)\sin(n\alpha)\,d(\alpha) \qquad (10)$$

From equation (10) and Fig.5

$$a_n=\frac{4}{\pi}\left[\int_{\alpha_1}^{\alpha_2} E_1\sin(n\alpha)\,d\alpha+\int_{\alpha_2}^{\alpha_3} E_2\sin(n\alpha)\,d\alpha+\cdots+\int_{\alpha_s}^{\frac{\pi}{2}} E_s\sin(n\alpha)d\alpha\right]$$

$$=\frac{4}{\pi}\left[-E_1\cos(n\alpha_2)+E_1\cos(n\alpha_1)-E_2\cos(n\alpha_3)+E_2\cos(n\alpha_2)-\cdots E_s\cos\left(n\frac{\pi}{2}\right)+E_s\cos(n\alpha_s)\right]$$

$$=\frac{4}{n\pi}[E_1\cos(n\alpha_1)+(E_2-E_1)\cos(n\alpha_2)+\cdots+(E_s-E_{s-1})\cos(n\alpha_s)] \qquad (11)$$

From Fig.4and Fig.5, the following relationship can be found

V1=E1, V2=E2 - E1 ...Vs= Es – Es-1 (12)

Substitute equation (12) into equation (11), we get

$$a_n=\frac{4}{n\pi}[V_1\cos(n\alpha_1)+V_2\cos(n\alpha_2)+\cdots+V_s\cos(n\alpha_s)]$$

(13)

Suppose the steps of equal heights,

$V_1= V^2$..... =Vs = E (14)

Therefore, for any s and odd n, an is given by

$$a_n=\frac{4E}{n\pi}[\cos(n\alpha_1)+\cos(n\alpha_2)+\cdots+\cos(n\alpha_s)]$$

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(or)

$$a_n = \frac{4E}{n\pi} \sum_{k=1}^{s} \cos(n\alpha_k) \quad (15)$$

Finally, the Fourier series of the quarter-wave symmetric s H-bridge cell multilevel inverter waveform written as follows:

$$V_{out}(\omega t) = \sum_{k=1}^{\infty} \left[\frac{4E}{n\pi} \sum_{k=1}^{s} \cos(n\alpha_k) \right] \sin(n\omega t) \quad (16)$$

Where

α_k Is the switching angle, which must satisfy the following condition

$$\alpha_1, \alpha_2, \alpha_3 \ldots\ldots\ldots, \alpha_s < \frac{\pi}{2}$$

s is the number of H-Bridge cells.
n is the odd harmonic order.
And E is the amplitude of dc voltages.

E. Circuit operation

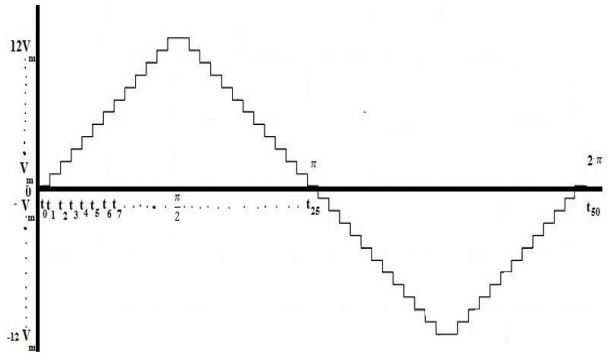

Fig.6 Operational waveform of proposed multilevel inverter

Fig.6 presents the ideal wave form of proposed multilevel inverter. Here Vm is the voltage applied by each voltage source. And the full cycle of proposed waveform is divided into 50 time intervals in order to satisfy the condition of 25 level output. Here time is denoted by t. Assume that load is a resistive load and is denoted by Re.

When t satisfies the condition that t0 ≤ t < t_1 in fig.6, the switches S1a to S6a, S2b to S6b are driven by gate source voltages, respectively. H-Bridge 1, H-Bridge 2, H- Bridge 3, H- Bridge 4, H- Bridge 5 and H-Bridge 6 are in forward freewheeling state and the output voltage is equal to 0. Because〖 s〗_1^ ı, s_2^ ı, s_3^ ı, s_4^ ı, s_5^ ı, s_6^ ı are on, the capacitors C1, C2, C3, C4, C5 and C6 are charged to Vin (Vdc1= Vdc2= Vdc3= Vdc4= Vdc5= Vdc6= Vin). The voltages on Bus1, Bus2, Bus3, Bus4, Bus5 and Bus6 are 0 as well.

When t satisfies the condition that t1 ≤ t < t_2 in fig.6, the switches S1a to S6a, S2b to S6b are driven by gate source voltages, respectively. H-Bridge 1is in forward conducting state and H- Bridge 2, H- Bridge 3, H- Bridge 4, H- Bridge 5 and H- Bridge 6 are in forward freewheeling state. Output voltage is equal to Vin. Because〖 s〗_1^ ı, s_2^ ı,s_3^ ı,s_4^ ı,s_5^ ı, s_6^ ıare on, the capacitors C1, C2, C3, C4, C5 and C6 are charged to Vin (Vdc1= Vdc2= Vdc3= Vdc4= Vdc5= Vdc6= Vin). The voltage on Bus1 is Vin and the voltages on Bus2, Bus3, Bus4, Bus5 and Bus6 is 0 as well.

When t satisfies the condition that t2 ≤ t < t_3 in fig.6, the switches S1a to S6a, S2b to S6b are driven by gate source voltages, respectively. H-Bridge 1, H-Bridge 2 is in forward conducting state and H- Bridge 3, H- Bridge 4, H- Bridge 5 and H- Bridge 6 are in forward freewheeling state. Output voltage is equal to 2Vin. Because〖 s〗_1^ ı, s_2^ ı,s_3^ ı,s_4^ ı,s_5^ ı, s_6^ ıare on, the capacitors C1, C2, C3, C4, C5 and C6 are charged to Vin (Vdc1= Vdc2= Vdc3= Vdc4= Vdc5= Vdc6= Vin). The voltage on Bus1, Bus2 is Vin and the voltages on Bus3, Bus4, Bus5 and Bus6 are 0 as well

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When t satisfies the condition that t3 ≤ t < t_4 in fig.6, the switches S1a to S6a, S2b to S6b are driven by gate source voltages, respectively. H-Bridge 1, H-Bridge 2, H- Bridge 3 are in forward conducting state and H- Bridge 4, H- Bridge 5 and H- Bridge 6 are in forward freewheeling state. Output voltage is equal to 3Vin. Because〖 s〗_1^ ı, s_2^ ı,s_3^ ı,s_4^ ı,s_5^ ı, s_6^ ıare on, the capacitors C1, C2, C3, C4, C5 and C6 are charged to Vin (Vdc1= Vdc2= Vdc3= Vdc4= Vdc5= Vdc6= Vin). The voltage on Bus1, Bus2, Bus3, is Vin and the voltages on Bus4, Bus5, Bus6 are 0 as well.

When t satisfies the condition that t4 ≤ t < t_5 in fig.6, the switches S1a to S6a, S2b to S6b are driven by gate source voltages, respectively. H-Bridge 1, H-Bridge 2, H- Bridge 3, H- Bridge 4 are in forward conducting state and H- Bridge 5 and H- Bridge 6 are in forward freewheeling state. Output voltage is equal to 4Vin. Because〖 s〗_1^ ı, s_2^ ı,s_3^ ı,s_4^ ı,s_5^ ı, s_6^ ıare on, the capacitors C1, C2, C3, C4, C5 and C6

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are charged to Vin (Vdc1= Vdc2= Vdc3= Vdc4= Vdc5= Vdc6= Vin). The voltage on Bus1, Bus2, Bus3 and Bus4 is Vin and the voltages on Bus5, Bus6 are 0 as well.

When t satisfies the condition that t5 ≤ t < t_6 in fig.6, the switches S1a to S6a, S2b to S6b are driven by gate source voltages, respectively. H-Bridge 1, H-Bridge 2, H- Bridge 3, H- Bridge 4, H- Bridge 5 are in forward conducting state and H- Bridge 6 is in forward freewheeling state. Output voltage is equal to 5Vin. Because⟦ s⟧_1^ ا, s_2^ ا,s_3^ ا,s_4^ ا,s_5^ ا, s_6^ اare on, the capacitors C1, C2, C3, C4, C5 and C6 are charged to Vin (Vdc1= Vdc2= Vdc3= Vdc4= Vdc5= Vdc6= Vin). The voltage on Bus1, Bus2, Bus3, Bus4 and Bus5 is Vin and the voltage on Bus6 is 0 as well.
When t satisfies the condition that t6 ≤ t < t_7 in fig.6, the switches S1a to S6a, S2b to S6b are driven by gate source voltages, respectively. H-Bridge 1, H-Bridge 2, H- Bridge 3, H- Bridge 4, H- Bridge 5 and H- Bridge 6 are in forward conducting state. Output voltage is equal to 6Vin. Because⟦ s⟧_1^ ا, s_2^ ا,s_3^ ا,s_4^ ا,s_5^ ا, s_6^ اare on, the capacitors C1, C2, C3, C4, C5 and C6 are charged to Vin (Vdc1= Vdc2= Vdc3= Vdc4= Vdc5= Vdc6= Vin). The voltage on Bus1, Bus2, Bus3, Bus4, Bus5 and Bus 6 is Vin.

When t satisfies the condition that t7 ≤ t < t_8 in fig.6, the switches S1a to S6a, S2b to S6b are driven by gate source voltages, respectively. H-Bridge 1, H-Bridge 2, H- Bridge 3, H- Bridge 4, H- Bridge 5 and H-Bridge 6 are in forward conducting state. Output voltage is equal to 7Vin. Because s1, s_2^ ا,s_3^ ا,s_4^ ا,s_5^ ا, s_6^ اare on, the capacitors C1 is discharging and C2, C3, C4, C5 and C6 are charged to Vin (Vdc1= Vdc2= Vdc3= Vdc4= Vdc5= Vdc6= Vin). The voltage on Bus1 is 2Vin and the voltages on Bus2, Bus3, Bus4, Bus5 and Bus 6 are Vin.

When t satisfies the condition that t8 ≤ t < t_9 in fig.6, the switches S1a to S6a, S2b to S6b are driven by gate source voltages, respectively. H-Bridge 1, H-Bridge 2, H- Bridge 3, H- Bridge 4, H- Bridge 5 and H-Bridge 6 are in forward conducting state. Output voltage is equal to 8Vin. Because s1, s2, s_3^ ا,s_4^ ا,s_5^ ا, s_6^ اare on, the capacitors C1, C2 are discharging and C3, C4, C5 and C6 are charged to Vin (Vdc1= Vdc2= Vdc3= Vdc4= Vdc5= Vdc6= Vin). The voltage on Bus1, Bus2 is 2Vin and the voltages on Bus3, Bus4, Bus5 and Bus 6 are Vin.

When t satisfies the condition that t9 ≤ t < t_10 in fig.6, the switches S1a to S6a, S2b to S6b are driven by gate source voltages, respectively. H-Bridge 1, H-Bridge 2, H- Bridge 3, H- Bridge 4, H- Bridge 5 and H-Bridge 6 are in forward conducting state. Output voltage is equal to 9Vin. Because s1, s2, s3, s_4^ ا,s_5^ ا, s_6^ اare on, the capacitors C1, C2, C3are discharging and C4, C5 and C6 are charged to Vin (Vdc1= Vdc2= Vdc3= Vdc4= Vdc5= Vdc6= Vin). The voltage on Bus1, Bus2 and Bus3 is 2Vin and also the voltages on Bus4, Bus5 and Bus 6 are Vin.

When t satisfies the condition that t10 ≤ t < t_11 in fig.6, the switches S1a to S6a, S2b to S6b are driven by gate source voltages, respectively. H-Bridge 1, H-Bridge 2, H- Bridge 3, H- Bridge 4, H- Bridge 5 and H-Bridge 6 are in forward conducting state. Output voltage is equal to 10Vin. Because s1, s2, s3, s4,s_5^ ا, s_6^ اare on, the capacitors C1, C2, C3, C4 are discharging and C5 and C6 are charged to Vin (Vdc1= Vdc2= Vdc3= Vdc4= Vdc5= Vdc6= Vin). The voltage on Bus1, Bus2, Bus3 and Bus4 is 2Vin and also the voltages on Bus5 and Bus 6 are Vin.

When t satisfies the condition that t11 ≤ t < t_12 in fig.6, the switches S1a to S6a, S2b to S6b are driven by gate source voltages, respectively. H-Bridge 1, H-Bridge 2, H- Bridge 3, H- Bridge 4, H- Bridge 5 and H-Bridge 6 are in forward conducting state. Output voltage is equal to 11Vin. Because s1, s2, s3, s4, s5, s_6^ اare on, the capacitors C1, C2, C3, C4, C5 are discharging and C6 is charged to Vin (Vdc1= Vdc2= Vdc3= Vdc4= Vdc5= Vdc6= Vin). The voltage on Bus1, Bus2, Bus3, Bus4 and Bus 5 is 2Vin and also the voltage on Bus 6 is Vin.

When t satisfies the condition that t12 ≤ t < t_13 in fig.6, the switches S1a to S6a, S2b to S6b are driven by gate source voltages, respectively. H-Bridge 1, H-Bridge 2, H- Bridge 3, H- Bridge 4, H- Bridge 5 and H-Bridge 6 are in forward conducting state. Output voltage is equal to 12Vin. Because s1, s2, s3, s4, s5, s6 are on and the capacitors C1, C2, C3, C4, C5, C6 are discharging (Vdc1= Vdc2= Vdc3= Vdc4= Vdc5= Vdc6= Vin). The voltages on Bus1, Bus2, Bus3, Bus4, Bus 5 and Bus6 are 2Vin.

The second quarter cycle is obtained in a similar manner, but the voltages here are gradually reducing from 12Vin to 0. And the second half cycle fromt25 at π onwards has similar active circuits as first half cycle (t25 –t50), but the direction of current is in

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opposite direction to provide negative voltage at the output. The relations of on state switches and the output voltage levels are given in Table I. When the operation enters a new state from an adjacent state, only one power switch changes between on and off. The output waveforms can be characterised by the following equation

$$\mathbf{THD}=\sqrt{\frac{\sum_{n=2}^{\infty} v_n^2}{v_1}}\times 100\%$$

Where, THD can be calculated by harmonic magnitudes.

III.DETERMINATION OF CAPACITANCE

From the analysis been seen above the capacitors are charged when they are in parallel with power source, and the capacitors are discharging when they are in series with the power source. The switch Si and Si' are driven alternatively during half of the output cycles. Therefore the driven frequency of Si and Si' is twice the frequency of output voltage.

The capacitance Ci is determined by the voltage ripple of Ci that denotes the voltage function of multilevel output. The larger capacitance has the fewer ripple voltage. The voltage fluctuation over a narrow scope has a smaller power losses and higher capacitor efficiency. The appropriated method of capacitance calculation is that the maximum voltage ripple is 10% of the maximum capacitor voltage [20].

Before calculating the capacitance of Ci, Two assumptions are made to simplify derivations: 1) the output load is pure resistive load, and 2) the same duration is given in each level of staircase output. Therefore the time points in Fig.6 are

$$t_0=0,\ t_1=\frac{1}{50}t_s,\ t_2=\frac{2}{25}t_s,\ t_3=\frac{3}{50}t_s,\ t_4=\frac{2}{25}t_s,\ t_5=\frac{1}{10}t_s,\ t_6=\frac{3}{25}t_s,\ t_7=\frac{7}{50}t_s,\ t_8=\frac{4}{25}t_s,\ t_9=\frac{9}{50}t_s,\ t_{10}=\frac{1}{5}t_s,\ t_{11}=\frac{11}{50}t_s,\ t_{12}=\frac{6}{25}t_s \quad (17)$$

Where, ts is period of output voltage driven by

$$t_s=\frac{1}{f_s} \quad (18)$$

Where, fs is the output voltage.

As shown in the above analysis, the longest discharging of C1is t7 to t19, the longest discharging of C2 is t8 to t18, the longest discharging of C3 is t9 to t17, the longest discharging of C4 is t10 to t16, the longest discharging of C5 is t11 to t15, and the longest discharging of C6 is t12 to t14.Therefore, Maximum discharge of C1 is QC1 and is defined as

$$Q_{c1}=\int_{t_7}^{t_{19}} sin(2\pi f_s t-\varphi)dt \quad (19)$$

Where the Iout is the amplitude of the output current iout and φ is the phase difference between the output voltage v0 and the current iout .If 1% ripple voltage is considered, QC1 should be less than 10% of the maximum charge of C1, i.e.

$$C_1\geq\frac{QC_1}{0.1V_{in}} \quad (20)$$

Similarly, Maximum discharge of C2 is QC2,

$$Q_{c2}=\int_{t_8}^{t_{18}} sin(2\pi f_s t-\varphi)dt \quad \text{And}$$

$$C_2\geq\frac{QC_2}{0.1V_{in}} \quad (21)$$

Maximum discharge of C3 is QC3,

$$Q_{c3}=\int_{t_9}^{t_{17}} sin(2\pi f_s t-\varphi)dt$$

$$\text{And } C_3\geq\frac{QC_3}{0.1V_{in}} \quad (22)$$

Maximum discharge of C4 is QC4,

$$Q_{c4}=\int_{t_{10}}^{t_{16}} sin(2\pi f_s t-\varphi)dt$$

$$\text{And } C_3\geq\frac{QC_3}{0.1V_{in}} \quad (23)$$

Maximum discharge of C5 is QC5,

$$Q_{c5}=\int_{t_{11}}^{t_{15}} sin(2\pi f_s t-\varphi)dt$$

$$\text{And } C_5\geq\frac{QC_5}{0.1V_{in}} \quad (24)$$

Maximum discharge of C6 is QC6,

$$Q_{c6}=\int_{t_{12}}^{t_{14}} sin(2\pi f_s t-\varphi)dt$$

$$\text{And } C_6\geq\frac{QC_6}{0.1V_{in}} \quad (25)$$

When the load is resistive, the voltage and the load current are in phase. The maximum discharge of capacitor is obtained in resistive load, because the peak load current is the midpoint of integration period. In other words, if the capacitance of Ci is derived in pure resistive load, it also maintains less voltage ripples in inductive load. The peak current of the capacitor Ci is derived by

$$I_{ci}=\frac{V_{in}-V_{Ci}-V_{dF}}{r_c+r_{on}+r_d} \quad (26)$$

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Where VCi is the voltage on capacitor Ci, VdF is the forward voltage drop of diode, rc is the equivalent resistance of capacitors, ron is the internal on state resistance of the switching device, and rd is the internal on state resistance of the diode. Because of small voltage difference of Vin and VCi, the peak current ICi is fewer for larger Ci. Thus, the larger capacitor is needed to cut down the undesirable peak current and prolong the capacitor lifetime.

The analysis of switching loss is similar to the traditional cascaded H-Bridge,While the capacitor losses consisting of ripple loss Prip and the conduction loss Pcond are newly introduced by proposed multilevel inverter. When the capacitor Ci is connected from series to parallel, the ripple is derived by the difference between the input voltage Vin and the capacitor voltage VCi. The voltage ripple of Ci is

$$\Delta V_{rip} = \frac{1}{C_i} \int_{t_-}^{t_+} i_{Ci}\, dt \qquad (27)$$

Table I
Relation between On-State Switches and Output Voltages

ON STATE SWITCHES	OUTPUT VOLTAGE(v)	CAPACITOR STATE
S_1 to S_6, S_{1a} to S_{6a}	$12V_m$	C_1 to C_6 discharging
S_1 to S_5, S_{1a} to S_{6a}	$11V_m$	C_1 to C_5 discharging, C_6 charging
S_1 to S_4, S_{1a} to S_{6a}	$10V_m$	C_1 to C_4 discharging, C_5, C_6 charging
S_1 to S_3, S_{1a} to S_{6a}	$9V_m$	C_1 to C_3 discharging, C_4 to C_6 charging
S_1, S_2, S_{1a} to S_{6a}	$8V_m$	C_1,C_2 discharging, C_3 to C_6 charging
S_1 , S_{1a} to S_{6a}	$7V_m$	C_1 discharging, C_2 to C_6 charging
S_{1a} to S_{6a}	$6V_m$	C_1 to C_6 charging
S_{1a} to S_{6a}, S_{6b}	$5V_m$	C_1 to C_6 charging
S_{1a} to S_{6a}, S_{6b},S_{5b}	$4V_m$	C_1 to C_6 charging
S_{1a} to S_{6a}, S_{6b} to S_{5b}	$3V_m$	C_1 to C_6 charging
S_{1a} to S_{6a}, S_{2b} to S_{6b}	$2V_m$	C_1 to C_6 charging
S_{1a} to S_{6a}, S_{2b} to S_{5b}	V_m	C_1 to C_6 charging
S_{1a} to S_{6a}, S_{1b} to S_{6b}	0	C_1 to C_6 charging
S_{2a} to S_{6a}, S_{1b} to S_{6b}	$-V_m$	C_1 to C_6 charging
S_{3a} to S_{6a}, S_{1b} to S_{6b}	$-2V_m$	C_1 to C_6 charging
S_{4a} to S_{6a}, S_{1b} to S_{6b}	$-3V_m$	C_1 to C_6 charging
S_{5a} , S_{6a}, S_{1b} to S_{6b}	$-4V_m$	C_1 to C_6 charging
S_{6a}, S_{1b} to S_{6b}	$-5V_m$	C_1 to C_6 charging
S_{1b} to S_{6b}	$-6V_m$	C_1 to C_6 charging
S_1, S_{1b} to S_{6b}	$-7V_m$	C_1 discharging, C_2 to C_6 charging
S_1, S_2, S_{1b} to S_{6b}	$-8V_m$	C_1,C_2 discharging, C_3 to C_6 charging
S_1 to S_3, S_{1b} to S_{6b}	$-9V_m$	C_1 to C_3 discharging, C_4 to C_6 charging
S_1 to S_4, S_{1b} to S_{6b}	$-10V_m$	C_1 to C_4 discharging, C_5, C_6 charging
S_1 to S_5, S_{1b} to S_{6b}	$-11V_m$	C_1 to C_5 discharging, C_6 charging
S_1 to S_6, S_{1b} to S_{6b}	$-12V_m$	C_1 to C_6 discharging

Where i_{Ci} is the transient current of the capacitor C_i, and the discharging interval is denoted by t_- and t_+. For C_1, t_- and t_+ are t_7 to t_{19}. Similarly we can write for all the capacitors. Thus, the loss from voltage ripple is resulted by

$$P_{rip} = \sum_{i=1}^{k} C_i \Delta V_{rip}^2 f_s \qquad (28)$$

Where k is the number of switched capacitors, and f_s is the frequency of output voltage. It is evident that the ripple loss is inversely proportional to the capacitor C_i. The conduction loss can be further calculated by

$$\boldsymbol{P_{COND} = 2f_s \sum_{i=1}^{k} \int_{t_-}^{t_+} r_c i_{Ci}^2 dt} \ \textbf{(29)}$$

The larger capacitor current leads to the large conduction loss. Lastly the losses from Sc's are given by the following equation

$$P_{SC} = P_{RIP} + P_{COND} \qquad (30)$$

Both the ripple loss and conduction loss are proportional to the frequency of output voltage and number of capacitors. It is concluded that a larger capacitor can improve efficiency prolong capacitor lifetime. The larger the capacitor, the higher the cost. Thus, a trade off cost and efficiency need to be taken into account.

IV. PERFORMANCE EVALUATION

The simulation based on matlab is performed for proposed inverter. The wave form s of output voltage v_0 is shown in fig.7 the following are the parameters are used for low power simulation. The voltage v_{in}=12v for each module, the module1 capacitor is c_1=100$\boldsymbol{\mu}$f, the module2 capacitor is

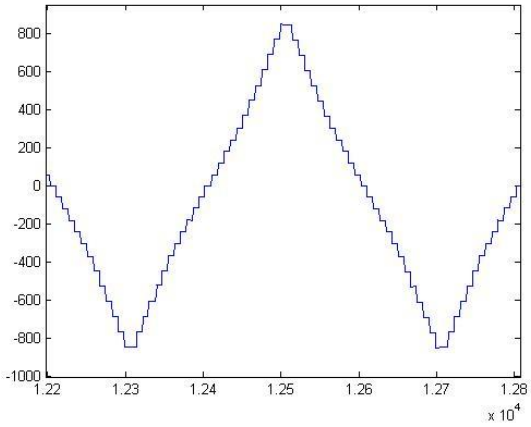

Fig.7 High Power Output Of Proposed 25-Level Inverter.

C_2=100$\boldsymbol{\mu}$F, the module3 capacitor is C_3=100$\boldsymbol{\mu}$F, the module4 capacitor is c_4=220$\boldsymbol{\mu}$f, the module5 capacitor is c_5=220$\boldsymbol{\mu}$f, the module6 capacitor is C_6=220$\boldsymbol{\mu}$F, the diodes d_1, d_2, d_3, d_4, d_5 and d_6 have 0.6v forward voltage drop and 50mΩ internal on state resistance and the load resistance is r_0= 12Ω. the following are the parameters are used for low power simulation. the voltage v_{in}=100v for each module, the module1 capacitor is c_1=300$\boldsymbol{\mu}$f, the module2 capacitor is

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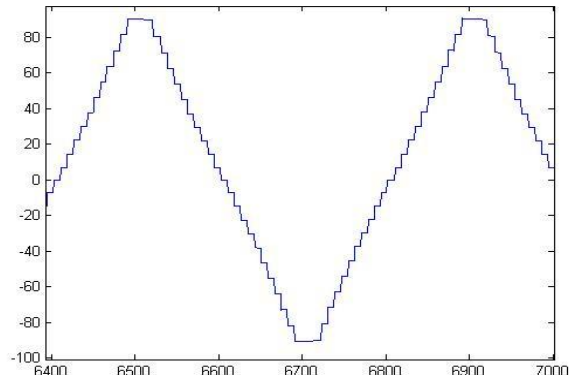

Fig.8 Low Power Output Of Proposed 25-Level Inverter.

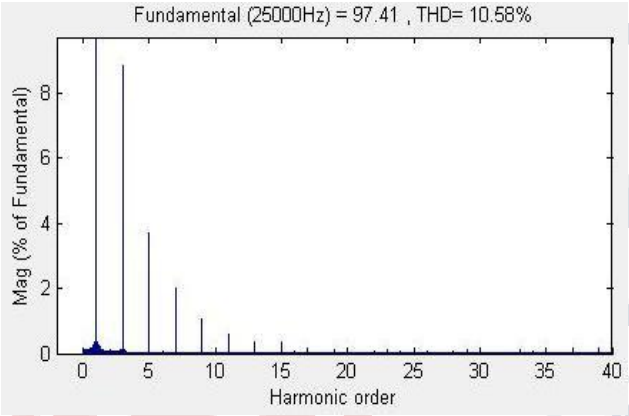

Fig.9 the of low power output of 25-level inverter.

c_2=300μf, the module3 capacitor is c_3=300μf, the module4 capacitor is c_4=560μf, the module5 capacitor is c_5=560μf, the module6 capacitor is c_6=560μf, the diodes d_1, d_2, d_3, d_4, d_5 and d_6 have 0.6v forward voltage drop and 50mΩ internal on state resistance and the load resistance is r_0= 12Ω. the output frequency is 25 khz. the waveforms of high power and low power are given in fig.7 and fig.8, respectively. so it is evident that proposed inverter can work at higher power. fig.9 and fig.10 gives the total harmonic distortions of low power output and high power output, respectively. the low power nine level output and thd of 9-level inverter is shown in fig.11 and fig.12 respectively. from the outputs of nine level and twenty five level multilevel inverters, it is clear that the 25-level output has a fewer higher order harmonics than the 9-level multilevel inverter output. The low power nine levels

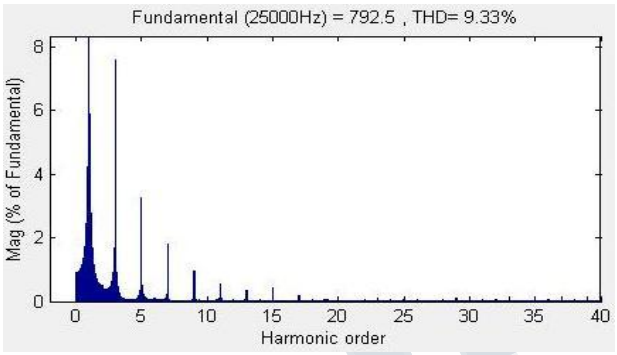

Fig.10 the of high power output of 25-level inverter

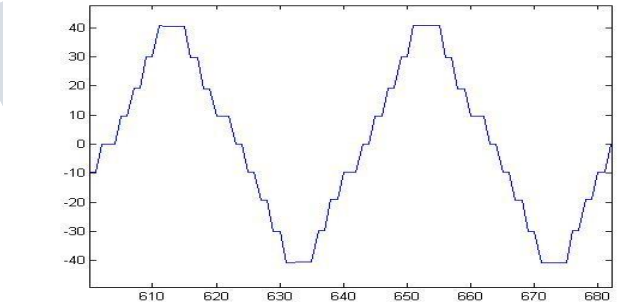

Fig.11 low power output of 9-level inverter

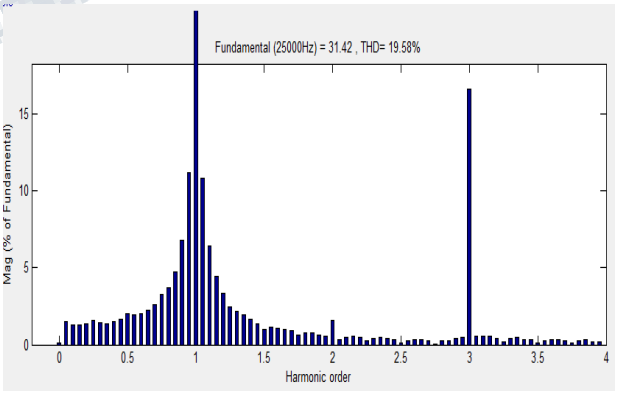

Fig.12 THD of 9-level output

Topology has the following parameters. V_{in}=12V, C_1=100μF with ESR 80mΩ, C_2=220μF with 50mΩ ESR, D_1&D_2 have 0.6V r_d and 50mΩ on state resistance, R_{on}=12Ω. The following table compares the THD of 9-level output and 25 -level output.

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Table II

Comparison of 9-level and 25-level outputs

	9-LEVEL	25-LEVEL
THD of low power output	19.58%	10.58%
THD of high power output	26.59%	9.33%

V. CONCLUSION

In this paper, A switched capacitor based multilevel inverter using stepped waveform technique was proposed. Both 9-level and 25- level inverter topologies are examined in depth. Compared with conventional cascaded multilevel inverter, the proposed inverter can greatly decrease the number of switching devices. A unique stepped wave technique was presented with low switching frequency and simple implementation. The accordant results of simulation results confirm the feasibility of proposed circuit and modulation method. Comparing with traditional cascaded H-Bridge multilevel inverter, the number of levels can be further increased by SC frontend. The harmonics are significantly cut down by in stair case output, which is partially remarkable due to simple and flexible circuit topology. Meanwhile, the magnitude control can be done by using appropriate PWM techniques and can be served as HF source with controlled magnitude and fewer harmonics. This paper analyzes 9-level and 25-level inverters. The method of analysis and design is also applicable to other members of proposed inverters. The proposed inverter is applied to grid-connected photovoltaic systems and electrical network of EV, because the multiple dc sources are available easily from solar panel, batteries, ultra capacitors and fuel cells.

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