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# A Novel Cascaded Two-Level H-Bridge Voltage Source Inverter Based STATCOM for High Power Applications

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***Abstract:*** **-- In this paper presents a var compensation by a cascaded two-level H-Bridge VSI based multilevel static compensator (STATCOM) using SVPWM. The topology consists of two voltage source inverters are connected in cascaded through a 3-phase transformer. The benefit of this topology is that by maintaining asymmetric voltages at the dc capacitors of the inverters, the levels in the waveform of output voltage can be increases. This results power quality (PQ) improved. The main object of this paper is balancing the dc link capacitor voltages of multilevel inverters during balancing and unbalancing conditions. This controller is controlling inverter voltage in such a way that either –ve sequence current flowing into the inverter is eliminated or reduces the unbalancing in the grid voltages. The performance of the control scheme during balanced and unbalanced conditions is analysed through MATLAB/SOMULINK.**

***Key Words*****: Dc link capacitor voltage balance, Power Quality (PQ), Multilevel voltage source inverters (VSI), Static Compensator, (STATCOM), Volt-Ampere Reactive (VAR), space vector pulse width modulation (SVPWM).**

## I. INTRODUCTION

The power quality is the major issue in the power systems. Power quality is improved in power system by using flexible ac transmission systems (FACTS) controller. The thyristor-controlled reactor (TCR), thyristor switched capacitors (TSC), static compensator (STATCOM), static var compensators (SVR), static synchronous series compensators (SSSC). Static synchronous compensator is a reliable reactive power controller compared to conventional var compensators. STATCOM provides active power oscillation damping, reactive power compensation, voltage regulation and flicker attenuation. [1].

STATCOM (Static Compensator) consists of a two-level Voltage Source Converter (VSC) are connected cascaded through a 3-phase transformer. The voltage source inverter converts the dc voltage across capacitors or dc storing devices into a set of 3-phase ac output voltages. These voltages are in phase and coupled with the ac system through the reactance of the coupling transformer. Suitable adjustment of the phase and magnitude of the static compensator output voltages allows effective control of active power and reactive power exchanges between the static compensator and the ac system. Such configuration allows the device to absorb or generate controllable active power and reactive power.

Static volt ampere reactive compensation by cascading multilevel level inverters is an effective solution for high-power applications [6], [7]. The topology consists of two standard two level H-Bridge VSI inverters connected in cascade through 3-phase transformer. The benefit of this topology is maintaining asymmetric voltages at the dc capacitor links of the inverters, the number of levels in the waveform of output voltage can be increased. This improves power quality. Therefore, overall control is simple compared to conventional multilevel inverters. Various volt ampere reactive compensation schemes based on this topology are reported in [3]–[5].

## II. POWER SYSTEM MODELLING AND DESCRIPTION

Fig.1. shows power system and static compensator model. This model represents the connection point of STATCOM in the power system.

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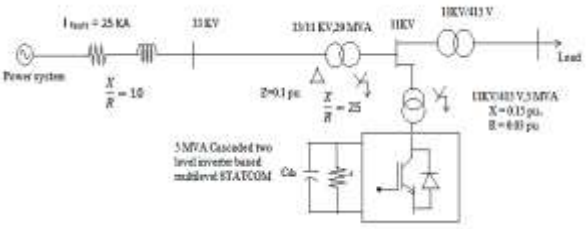

*Fig.1 Power system and the STATCOM model*

The schematic diagram of cascaded two-level inverter based multi-level static compensator is shown in Fig.2. The low-voltage (LV) side of a transformer connected to inverter and high voltage (HV) side of a transformer is connected to grid.

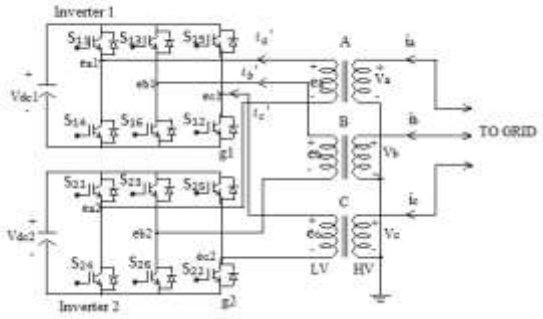


*Fig.2. Cascade two-level inverter based STATCOM*

A Multi-level inverter uses the insulated gate bipolar transistors switches in high power applications. The two inverters i.e inverter 1 and inverter 2 are connected in cascaded through 3-phase transformer. $V_{dc1}$ and $V_{dc2}$ are the dc link capacitors voltages of inverter 1 and inverter 2. The dc link capacitor voltages of inverters are regulated at different level to obtain four –level operation.

Fig.3. shows the equivalent circuit of cascaded two-level H-Bridge inverter based multilevel based STATCOM. In the Fig.3, the 3- phase RMS source voltages $V_a'$, $V_b'$ and $V_c'$ referred to the low-voltage side of the transformer.

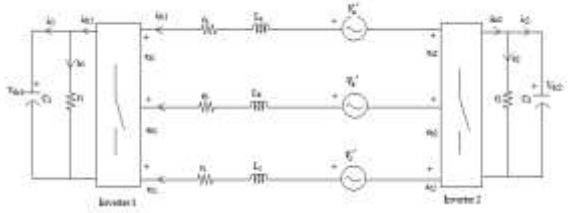

*Fig.3 Equivalent circuit of two-level H-Bridge inverter based STATCOM*

### A. *Phase Equivalent Circuit*

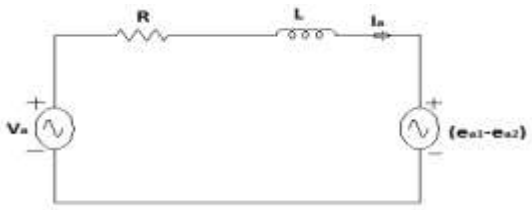


*Fig.4. Equivalent circuit of phase a*

Equivalent circuit of phase 'a' is shown in Fig.4.in which figure $v_a'$ is the RMS source voltage, R is the total losses in the system, L is the leakage inductance of the transformer, ($e_{a1}$-$e_{a2}$) is the voltage across primary side of the transformer of inverter 1 and inverter 2.

Applying KVL to the loop

$$-v_a' + R_a I_a' + L_a \frac{di_a'}{dt} + (e_{a1}\text{-}e_{a2}) = 0 \qquad (1)$$

Similarly for 'b' and 'c' phases

$$-v_b' + R_b I_b' + L_b \frac{di_b'}{dt} + (e_{b1}\text{-}e_{b2}) = 0 \qquad (2)$$

$$-v_c' + R_c I_c' + L_c \frac{di_c'}{dt} + (e_{c1}\text{-}e_{c2}) = 0 \qquad (3)$$

Assuming resistances $R_a = R_b = R_c = R$ and inductances $L_a = L_b = L_c = L$, the above equations can be written in mathematical model form as,

$$\begin{bmatrix} \frac{di'_a}{dt} \\ \frac{di'_b}{dt} \\ \frac{di'_c}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r}{L} & 0 & 0 \\ 0 & \frac{-r}{L} & 0 \\ 0 & 0 & \frac{-r}{L} \end{bmatrix} \begin{bmatrix} i'_a \\ i'_b \\ i'_c \end{bmatrix} + \frac{1}{L} \begin{bmatrix} V'_a - (e_{a1} - e_{a2}) \\ V'_b - (e_{b1} - e_{b2}) \\ V'_c - (e_{c1} - e_{c2}) \end{bmatrix} \qquad (4)$$

The equation (4) is known as mathematical model in the stationary reference frame of cascaded two-level voltage source inverter based STATCOM. To control both the active and reactive currents independently, this stationary reference frame model can be converted into rotating reference frame model. The source voltage of q-component is set to be zero so

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that the source voltage of d-component can be aligning with the synchronously rotating reference frame.

The dynamic model in the synchronously rotating reference form is give as

$$\begin{bmatrix} \frac{di_d'}{dt} \\ \frac{di_q'}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r}{L} & \omega \\ -\omega & \frac{-r}{L} \end{bmatrix} \begin{bmatrix} i_d' \\ i_q' \end{bmatrix} + \frac{1}{L} \begin{bmatrix} v_d' - (e_{d1} - e_{d2}) \\ -(e_{q1} - e_{q2}) \end{bmatrix} \quad (5)$$

Here $v_d'$ is direct (d)-axis voltage component of ac source and $i_d'$, $i_q'$ are d-axis and q-axis current components of cascaded two-level voltage source inverter.

### *B. Proposed Control Strategy*

Fig.5. shows control block diagram of circuit. The d-axis and q-axis voltages can be controlled as follows

$$e_d^* = -x_1 + \omega L i_q' + v'_d \quad (6)$$

$$e_q^* = -x_2 - \omega L i_d' + v'_q \quad (7)$$

Here $e_d^*$ and $e_q^*$ are d-axis and q- axis reference voltage components of inverters. The parameters $x_1$ and $x_2$ are known as control parameters and these can controlled as

$$x_1 = \left(k_{p1} + \frac{k_{i1}}{s}\right)\left(i_d^* - i_d'\right) \quad (8)$$

$$x_2 = \left(k_{p2} + \frac{k_{i2}}{s}\right)\left(i_q^* - i_q'\right) \quad (9)$$

Where $i_d^*$ is the direct (d)-axis reference current and is given by

$$i_d^* = (k_{p3} + \frac{k_{i3}}{s})[(V_{dc1}^* + V_{dc2}^*) - (V_{dc1} + V_{dc2})] \quad (10)$$

Where $V_{dc1}^*$ and $V_{dc2}^*$ are the reference voltages of dc-link capacitors of inverter 1 and inverter2. $V_{dc1}$ and $V_{dc2}$ are the actual dc link voltages of inverter 1 and inverter 2.reference reactive current component i.e q-axis component $i_q^*$ is obtained either from load, when used for load compensation [2] or from voltage regulation loop when used in transmission lines.

Fig.5. Shows that the three phase voltages $v_a$, $v_b$, $v_c$ are given to phase-locked loop (PLL) to generate the unit signals $\cos \omega t$ and $\sin \omega t$. Phase lock loop or phase locked loop (PLL) is a type of control system, which is used to generate output signal to match the phase of input signal. These unit signals are used to transform the converter currents $i_a'$, $i_b'$, $i_c'$ into synchronously rotating reference form currents. So that it is easy to control reactive and active current components. These currents consist of large switching frequency ripples and which are eliminated by using low-pass filters (LPF). The reference voltages to the converter are $e_d^*, e_q^*$ are generated from controller using $(V_{dc1}^* + V_{dc2}^*)$ and $i_q^*$. The inverter supplies desired reactive component of current $i_q^*$ and draws active component of current $i_d'$ by considering these reference current components. Which can be further used to regulate total dc-link voltage $V_{dc1}^* + V_{dc2}^*$ of the inverter. Due to these unequal dc-link capacitor voltages, the regulation of this dc-link voltage becomes difficult. For effective control of total dc-link voltage, an additional control method is required. The main disadvantage of this cascaded multi-level inverter based STATCOM is control of individual dc-link voltages is more difficult.

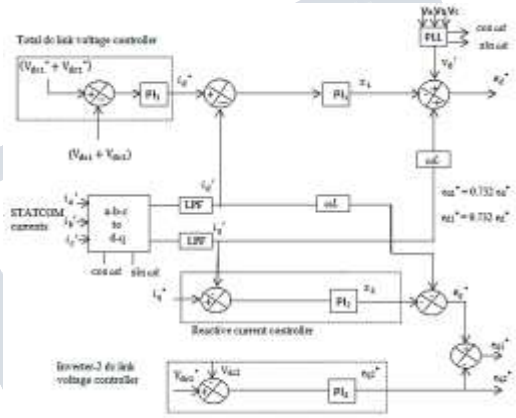


*Fig.5. Control circuit diagram*

### *C. DC-Link Balance Controller*

The total dc-link balance controller is used to provide magnitude and phase of resultant voltage supplied by the cascaded inverter. This is given by $e_I \angle \delta$. In which $e_I$ represents the magnitude of d-axis, q-axis voltage components and $\delta$ represents the phase angle of the respective components.

$$e_I = \sqrt{e_d^2 + e_q^2} \text{ and}$$

$$\delta = \tan^{-1}\left((e_q)/(e_d)\right) \quad (11)$$

The active power sharing between the inverter and grid is depends on angle $\delta$.From the figure, the reference voltage components of q-axis of the two inverters $e_{q1}^*$, $e_{q2}^*$ is obtained as

$$e_{q1}^* = e_q^* - e_{q2}^* \quad (12)$$

$$e_{q2}^* = \left(k_{p4} + \frac{k_{i4}}{s}\right)(V_{dc2}^* - V_{dc2}) \quad (13)$$

$$V_{dc1} = 0.732\ V_{dc} \quad (14)$$

$$V_{dc2} = 0.268\ V_{dc} \quad (15)$$

The d-axis voltage component $e_d^*$ is shared between inverter1 and inverter2, to regulate the dc-link voltages of inverter1 and inverter2 proportional to their individual dc-link voltages.

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$e_{d1}^{*} = 0.732\ e_{d}^{*}$ (16)

$e_{d1}^{*} = 0.732\ e_{d}^{*}$ (17)

The power transfer to inverter1 is indirectly controlled and for inverter2, power transfer is directly controlled.The control circuit uses the sinusoidal pulse width modulation (SPWM) technique to generate gate signals from the obtained reference voltages. The reference voltages of two inverters are in phase opposition so that harmonic spectrum will be appeared at double the switching frequency.

### *D. Unbalanced Condition*

The dc link voltages of inverters consist of double supply frequency components, causes third harmonic components in the ac side of inverter. Whenever load becomes unbalanced or asymmetric fault occurs, the ac side voltage of inverter becomes unbalanced, causes negative sequence voltages appeared in the supply voltage. Therefore large negative sequence currents will flow through inverter and it may leads to trip of STATCOM. Therefore when unbalance occurs STATCOM needs to supply these currents or should eliminate the unbalance in the supply voltages, to prevent inverter trip.

The reference voltage components of inverter is given by

$$e_{dn}{}^{*} = -x_3 - \omega L i_d^{'} + v'_{dn}$$

$$e_{qn}{}^{*} = -x_4 - (-\omega L) i_{dn}^{'} + v^{'}{}_{qn} \qquad (19)$$

## III. SIMULINK MODEL OF THE SYSTEM

The computer simulation using MATLAB/Simulink for multi-level statcom for high power applications using sinusoidal pulse width modulation is shown in Fig.8 & Fig.9. Table I shows system parameter used in simulation.

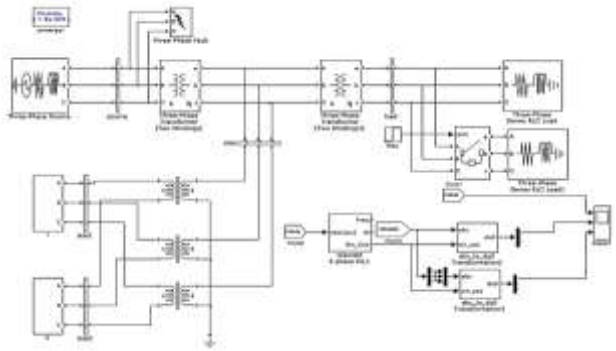

*Fig.8. Simulink model of the system*

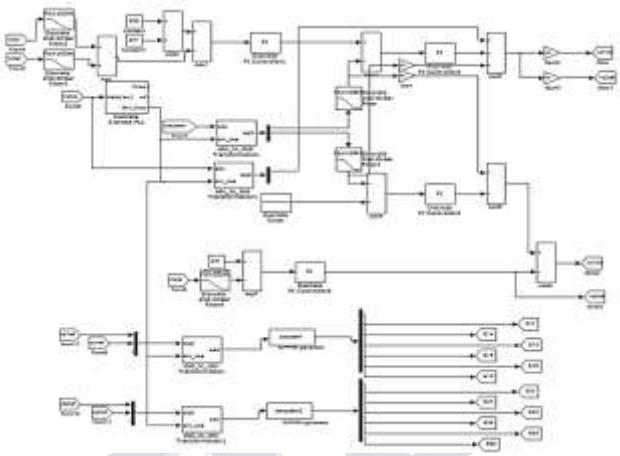

*Fig.9. Control circuit*

***Table. I: Simulation Parameters***

| | |
|---|---|
| Rated power | 5 MVA |
| Transformer voltage rating | 11KV/400 |
| AC supply frequency, f | 50 HZ |
| Inverter-1 dc link voltage, Vdc1 | 659 V |
| Inverter-2 dc link voltage, Vdc2 | 241 V |
| Transformer leakage reactance, $X_l$ | 15% |
| Transformer resistance, R | 3% |
| DC link capacitances, $C_1$, $C_2$ | 50 Mf |
| Switching frequency | 1200 Hz |

## IV. SIMULATION RESULTS

### *A. Reactive power control*

Fig.10 shows the waveforms of source voltage and inverter current, DC capacitor-link voltage of two inverters in the reactive power control case.

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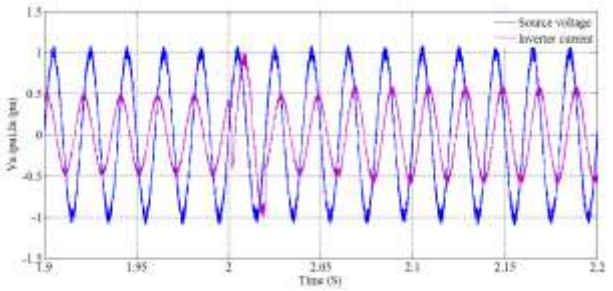

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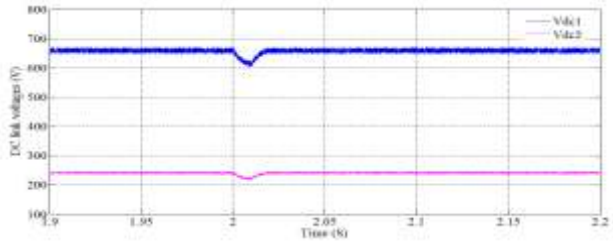


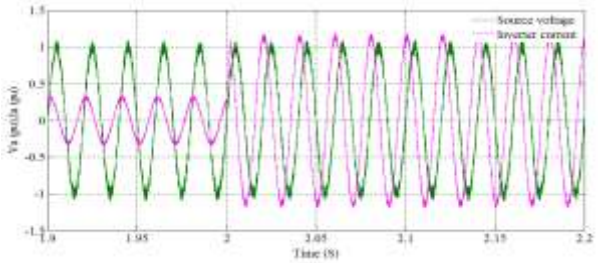
**(b)**

***Fig.10. a) Source voltage and Inverter current b) DC capacitor-link voltages of two inverters***

In this case reactive power is controlled by setting $i_q^*$ i.e reference reactive current component at a particular reference value. Initially $i_q^*$ is set at 0.5 p.u. At t=2.0 s, $i_q^*$ is changed from 0.5 to -0.5. Dc capacitor-link voltage of two inverters are regulated during the STATCOM modes are changed.

### *B. Load compensation*

Fig.11 shows the waveforms of source voltage and inverter current, DC capacitor-link voltage of two inverters in the load compensation case. In this case, reactive power of the load is compensated by the STATCOM. Initially STATCOM gives the current of +0.5 p.u. When load current increases at t=2.0 s, STATCOM gives more than +0.5 p.u. Therefore load compensation is effectively achieved by the STATCOM. The DC-link voltages of two inverters $V_{dc1}$ and $V_{dc2}$ are controlled at their respective values when STATCOM operating modes are changed.



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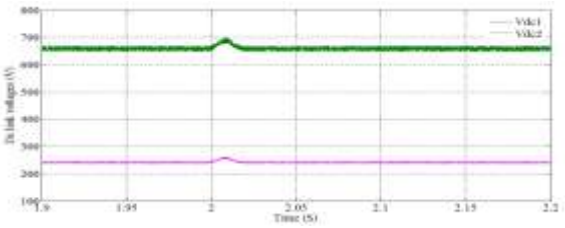
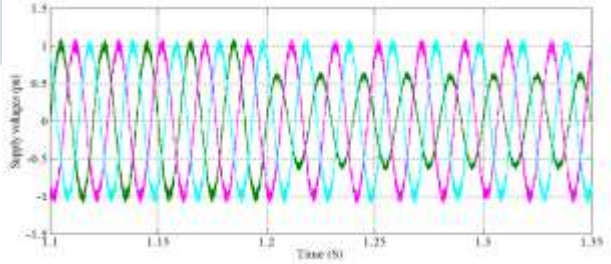


**(b)**

***Fig.11. a) Source voltage and inverter current b) DC-link voltages of two inverters***

### *C. Operating during the fault condition*

Fig.12 shows the waveforms of grid voltages on LV side of the transformer, during the fault condition. In which, a single line to ground fault is created at 1.2s and cleared after 200 ms on A phase of HV side of the 33/11 kv transformer. The corresponding d-q axis currents of the inverter are shown. The fault currents are controlled at their respective values i.e at zero.



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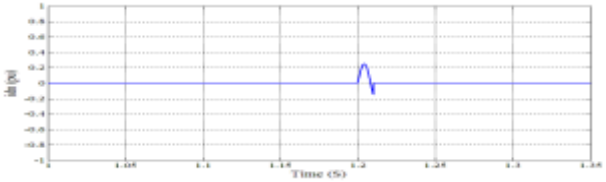

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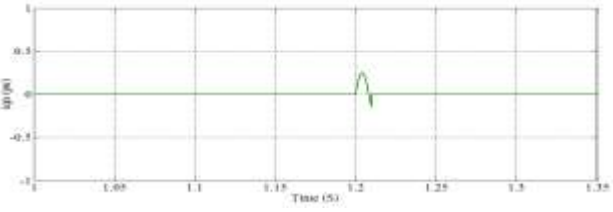

**(c)**

***Fig.12. a) Grid voltages on the LV side of the transformer b) d-axis negative sequence current component c) q-axis negative sequence current component***

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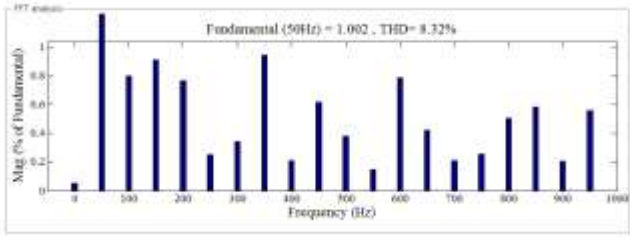
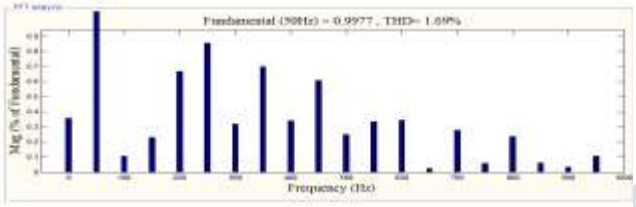
## FFT ANALYSIS

The frequency spectrum of different signals is obtained by this FFT analysis.




**(a)**




**(b)**

***Fig.12. FFT Analysis showing THD of load voltage a) with SPWM b) with SVPWM***

Total harmonic distortion is 8.32% with SPWM and THD is 1.69% with SVPWM.

## V.CONCLUSION

The balancing dc-link capacitor voltage of the cascaded H-Bridge multilevel inverter based statcom is a major issue. In this paper simple var compensation using a cascaded two level H-Bridge voltage source inverter based multilevel static compensator (STATCOM) is proposed. The scheme ensures regulation of dc link voltages of inverter at a asymmetrical levels and reactive power compensation. The main object of this paper is balancing the dc link voltages of multilevel inverters during balancing and unbalancing conditions. This controller is controlling inverter voltage in such a way that either –ve sequence current flowing into the inverter is eliminated or reduces the unbalancing in the grid voltages. SVPWM technique reduces the THD value of load voltage from 8.32% to 1.69%. Thus power quality is improved with Var compensation. The performance of the control scheme during balanced and unbalanced conditions is analysed through MATLAB/SOMULINK.

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