ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 2, Issue 12, December 2016

New Cascaded H-Bridge Multilevel Inverter Topology WithReduced Number of Switches

[1] Baishali Bhattacharjee [2] Mr. Tilok Boruah [3] Dr. Chhotan Sahu
[1] M.E Student [2] Assistant Professor [3] Professor
[1][2][3] EE Dept Jorhat Engineering College Jorhat, Assam

Abstract: **With the demand for high power inverter unit, multilevel inverter has been attracting extensive attention from academic as well as industry.The significant advantages of multilevel configuration are voltage sharing both statically and dynamically, and hence the quality of output voltage improves with the number of voltage steps with less harmonic contents.Though multilevel inverter has several advantages, it has drawbacks like for higher levels more number of semiconductor switches are needed which leads to huge size and high cost of the inverter. This paper deals with a novel seven level cascaded multilevel inverter.This topology reduces the complexity and overall size of the system which in turn reduces the harmonics and cost of the entire system.A seven level inverter simulation is carried with the implementation of PWM techniques.The effectiveness of the proposed inverter is adequately validated by softwaresimulation.Further comparison of the proposed topology with the existing topologies exemplifies the efficiency of the proposed topology.**

Keywords:-Multilevel inverters; PWM technique; Total harmonic distortion.

I. INTRODUCTION

The multilevel inverters have drawn greater interest in the power industry because of smooth out wave form, compact size etc.The inverter present a new set of aspects that are well suited to employ in reactive power compensation. It may be simple to generate a high voltage, high power inverter with the multilevel structure because of the way in which device voltage stress is managed in the power structure. A multilevel inverter is a power electronic interface that synthesizes a desired output voltage from several DC voltages as inputs. The research and development for these types of converters are gaining popularity especially for high power and high voltage applications due to the reduction in THD. Due to this the size of the passive filter will be smaller making the overall system compact. In addition to this, it produces output waveforms with a better harmonic spectrum, hence improved power quality and also has good electro-magnetic compatibility. Conventional multilevel inverters include diode clamped converter, flying capacitors, cascaded H-bridge. The cascaded H-bridge and the diode clamped are the most popularly hardware implemented topologies at present, especially in the growing technological field of renewable energy.

The initial inverters developed were only of two levels. The technology got advanced and multi level inverters were developed which can produce a desired output of different voltage levels from many input DC voltage sources. As the number of levels increase, the output attains near sinusoidal wave shape reducing the harmonics. The more the number of levels, the lesser is the harmonic content. Hence MLIs are becoming popular in applications where high voltage and high power are used. The disadvantage of MLI is that it involves many switches which require corresponding gate drive circuitry. This in turn increases the expenditure. Therefore the reduction in number of switches is essential.

II.CONVENTIONAL CASCADED MULTILEVEL INVERTER

A cascaded multilevel inverter uses set of series connected full-bridge inverters with separate DC sources in a modular setup to create the stepped waveform. A full bridge inverter is in itself a 3 level cascadedmultilevel inverter and every module added in cascade to that extends theinverter with twomore voltage levels, which then increases the number of steps in the waveform. A typical 5-level for a single phase leg is shown below. One can observe from here that it requires 8 switches. For a 7-level inverter model, it uses 12 switches, whereas the proposed model uses only 8.

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 2, Issue 12, December 2016

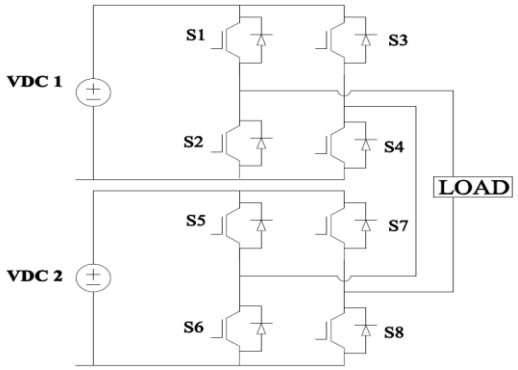

Figure1. Typical 5-level cascaded multilevel inverter circuit [2]

III.PROPOSED CASCADED MULTILEVEL INVERTER

General Description

The proposed multilevel topology is a hybrid multilevel inverter, which separates the output of the multilevel inverter into two parts. One part is named level generation part and it is responsible for level generating in positive polarity. The other part is called polarity generation part. The H-bridge is responsible for generating the polarity of the output voltage. H-bridge consisting of four switches and these switches are operating at fundamental frequency. The proposed seven levels inverter is shown in Fig. 2. As can be seen, it requires eight switches and three isolated sources. The main idea of this proposed topology as a multilevel inverter is that the left side in Fig. 2 generates the required output levels (without polarity) and the right side of the circuit (H-bridge inverter) decides about the polarity of the output voltage.The proposed system consists of a normal H bridge inverter and some auxiliary switches. A stepped waveform is generated at the output according to how the sources are being connected to the load. The H-Bridge is operated normally to generate alternating voltage output. During positive half cycle, switches M1 and M2 are turned on and the level selecting switches are operated to get different voltage levels. To generate the negative half cycle, switches M3 and M4 are conducting while the level selecting switches are operated to get a staircase voltage at the output. To obtain the first level, the dc source V1 must be connected to the load. To generate the second level, both V1 and V2 must be connected to the load. The rest of the sources are also connected in steps to the load in similar manner. The switches are controlled in such a way that respective sources are connected to the load during desired time intervals.

In the proposed topology the total switch count is 8 for a seven level multilevel inverter, in case of a conventional cascaded multilevel inverter it would be 12. Number of switches and gate driver circuits reduced in this topology so reducing the complexity of the overall circuit. It reduces the installation area and consequently the cost of the whole setup.

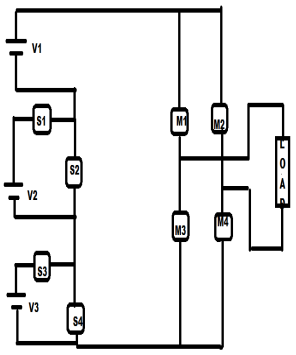

Figure2. Proposed cascaded multilevel inverter

For the cascaded H-bridge used in the proposed model, we have some mathematical design which are stated as : Say ,Vs = input voltage to the inverter circuit Then for first half cycle i.e, when M1 and M4 are the conducting switches we have :

$Vs = Ri + L \frac{di}{dt}$

Taking Laplace Transform we have,

$\frac{V_s}{s} = R.I(s) + Ls.I(s)$

$= I(s) [R + Ls]$

Again, we have

$i(t) = \frac{V_s}{R}(1 - e^{-\frac{R}{L}t})$ ----------(0 < t < T/2)

$andi(T/2) = \frac{V_s}{R} (1 - e^{-\frac{R}{2L}T})$ --------(t= T/2)

Similarly, for second half cycle i.e, when M2 and M3 are the conducting switches we have :

$-Vs = Ri + L \frac{di}{dt}$

And, $i(t) = - \frac{V_s}{R} + \frac{V_s}{R} (2 - e^{-\frac{2T}{2L}}) e^{-\frac{R}{L}t}$

Also,

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 2, Issue 12, December 2016

$V_o = \frac{2V_s}{\pi}\sin\omega t$ and $V_o\,(rms) = \frac{2V_s}{\sqrt{2}.\pi}$

And $I_o = \frac{V_o}{R}$

Fundamental component of I_o (i) = $\sqrt{2} * I_0$

Also, $I_s = \frac{\sqrt{2}.I_o}{\pi}$

Switching Sequence

Switching sequences in the proposed multilevel inverter are simpler as compared to conventional topologies. There is no need to control negative cycle so it does not generate negative pulses. Thus, there is no need for extra conditions for controlling the negative voltage. In table.1.shows the switching sequence of the proposed topology. In this, the switching transition is minimum during each mode transfer so there is a reduction in the switching loss.

TableI. Switching Sequence of the Proposed Topology

SWITCHES LEVELS	S1	S2	S3	S4
VDC	OFF	ON	OFF	ON
2VDC	ON	OFF	OFF	ON
3VDC	ON	OFF	ON	OFF

Modes of Operation

The output voltage of the proposed multilevel inverter has seven levels (VDC,2VDC,3VDC,0,-VDC,-2VDC,3VDC) according to the switching states of the inverter. The output voltage changes its value from zero to maximum voltage and the modes are same when the output changes from maximum to zero. The four operating modes are shown in respective figures.To produce a staircase voltage at the output the switches must be turned ON and OFF in a particular sequence, so that the voltage sources will get connected to the load in a desired manner.

Mode-1:The switches S2 and S4 are turned ON. The source voltage V1 is getting connected to the load as shown in Fig.3. mode1.M1 and M2 are turned ON to get the positive half cycle. All the other switches are kept off.

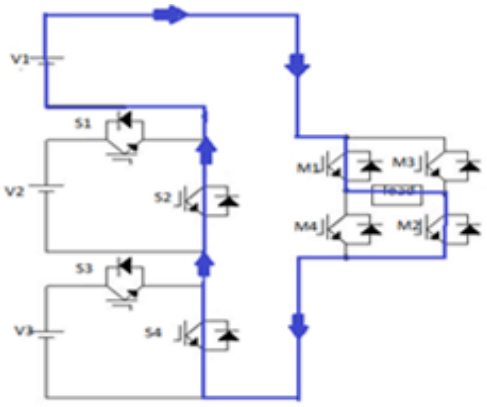

Figure3. Mode1 operation

Mode-2: The switches S1 and S4 are on during this time duration and source voltage 2VDC is connected to the load. All other switches are in OFF position.

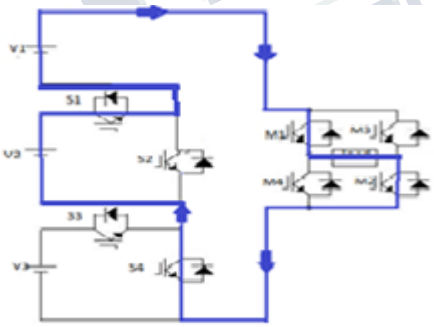

Figure.4 Mode2 operation

Mode-3: In this mode, S4 is turned OFF and S3 is turned ON. The output 3VDC is applied to the H-bridge.The switches which are conducting in the H-bridge are M1 and M2.

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 2, Issue 12, December 2016

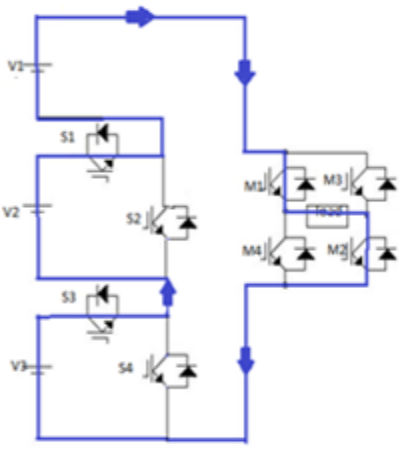

Figure5. Mode3 operation

Mode-0: It is a special mode which will develop a zero voltage level at the output. This mode is achieved with the help of H-bridge.Normally,M1 and M2 will be conducting simultaneously to generate the positive half cycle of the output. But if the switching pulse to M2 is delayed for a small time interval, the load inductance will try to maintain the current direction through it and as a result, the current will flow through the anti parallel diode of M3.During this freewheeling period, the voltage across the load is zero. Therefore the load freewheeling can be utilized to generate a zero voltage level. After reaching the maximum output, the level selection switches are operated in the reverse order to reach the zero level again. The operation of the level selection switches are the same for both positive and negative half cycles of the output. The only difference is that instead of switchesM1 and M2, switches M3 and M4 are conducting in the H-bridge for generating the negative half cycle.

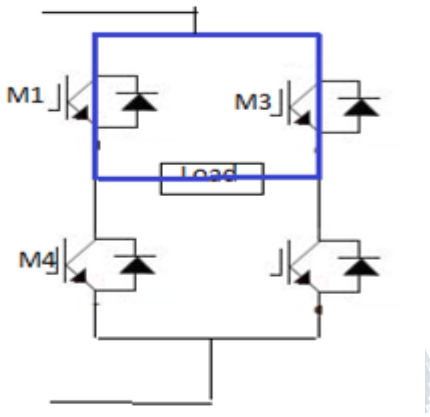

Figure6. Mode0 operation

IV.PWM TECHNIQUES

There are two schemes of carried based modulation. They are phase shifting and level shifting methods. Phase shifting scheme produces higher amount of total harmonic distortion when compared to level shifting scheme.Therefore level shifting is taken into consideration.Level shifting scheme is further divided into three schemes.Phase disposition, phase opposition disposition, alternate phase opposition disposition. This paper worked on phase opposition disposition scheme for the pulse generation for both switching topologies.

Phase Disposition(PD)

All the carrier (triangular) waveforms are in phase and it is intersected with the sinusoidal waveform to produce the seven level staircase waveform .The frequency of the sinusoidal wave is 50Hertz and the magnitude is 0.8V.The frequency of the carrier wave is about 20times of the frequency of the sinusoidal wave .The frequencies of the carrier and sinusoidal waveforms is same for two modulation techniques discussed in this paper. The diagrammatic representation is shown in figure 7.

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 2, Issue 12, December 2016

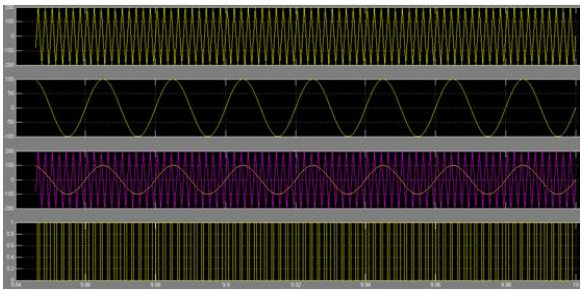

Figure7.Phase Disposition PWM

V. MATLAB/SIMULINK MODEL AND SIMULATION RESULTS

The simulation case study has been carried out software to validate the result. Fig.8.showsthe simulation model of the proposed topology where the total harmonic distortion is analyzed. To generate the seven level output voltage, eight MOSFETs and three DC power source of 12 Volts are used. Pulses are generated by using pulse widthmodulation method.The simulated Output voltage is shown in Fig.9.

Parameters	Diode clamped multilevel inverter	Flying capacitor multilevel inverter	Cascaded multilevel inverter	Proposed topology
No. of switches	10	10	12	8
No. of diodes	8	--	--	--
No. of capacitors	6	14	--	--

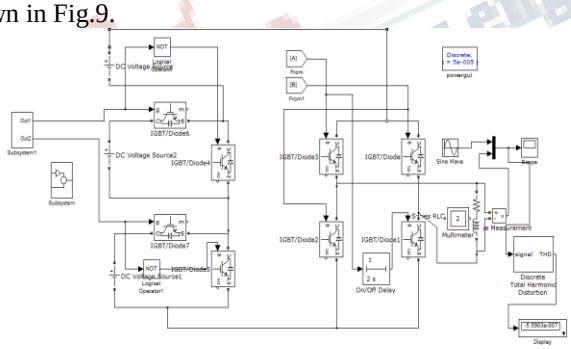

Figure8. Simulation model of proposed system

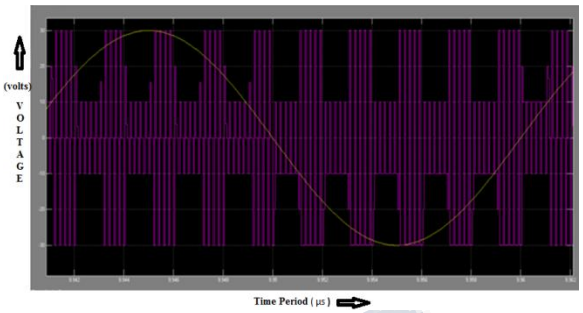

Figure9. Voltage waveform of proposed topology

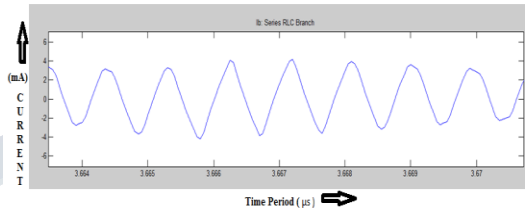

Figure10. Current waveform of the proposed topology

Total harmonic distortion (THD)of the proposed topology is -2.5031e-006 without using the LC filter.The current waveform of the proposed multilevel inverter without output filter is shown in Fig.10.

VI.COMPARISON

Compared to other topologies the proposed topology has many advantages. The proposed topology does not have any voltage unbalancing problems as in flying capacitor type topology. Ithas much more reduced no of switches compared to cascaded topology. A single H bridge can generate 3 voltage levels: +VDC,0, -VDC. Therefore 7-level multilevel inverter requires 12 switches in cascaded topology.The proposed topology requires 8 switches only. It does not need any auxillary devices like clamping capacitor or clamping diodes.The comparison between different topology is shown Table II % reduction in switches = 33.3%. Since there is a considerable reduction in number of switches, the various losses associated with the switches will also be reduced.

TableII. Comparison of Topologies

VII.CONCLUSION

In this paper a new topology of the cascaded multilevel inverter has been shown to produce an increased stepped output with less number of semiconductor switches. With fewer switches, controlling the overall circuit becomes

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 2, Issue 12, December 2016

less complex, the size, installation area reduces and THD are reduced as compared to conventional topologies Thecircuit design is validated usingsimulationsoftware.Phase disposition level shifting method is followed for the pulse generation for the topology.

REFERENCES

[1] P.Thongprasri "A 5 level 3 phase cascaded hybrid multilevel", International Journal of Computer and Electrical Engineering (Volume 3 No.6 Dec 2015).

[2] M. Kavitha,A. Arunkumar , N. Gokulnath , S. Arun "New Cascaded H-Bridge Multilevel Inverter Topology with Reduced Number of Switches and Sources" Volume 2, Issue 6 (Sep-Oct. 2012).

[3] A. Nabae, T. Isao, and A Hirofumi, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Trans. Ind. Applicat.*, vol. IA-17, No.5. pp. 518-523, 1981.

[4] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *23rd Annual IEEE Power Electronics Specialists Conference*, pp. 397-403, 1992.

[5] P. W. Hammond, "A new approach to enhance power quality for medium voltage AC drives," *IEEE Trans. Ind. Applicat.*, vol. 33, pp. 202-208, 1997.

[6] Brendan Peter McGrath, and Donald Grahame Holmes, "Multicarrier PWM Strategies for Multilevel Inverters", *IEEE Trans. on Industrial Electronics*, Vol. 49, No. 4, Aug. 2002.

[7] Andreas Nordvall, "Multilevel Inverter Topology Survey", Master of Science Thesis in Electric Power Engineering, Department of Energy and Environment, Chalmers University of Technology, Goteberg, Sweden, 2011.

[8] Ian F. Crowley, and Ho Fong Leung, "PWM Techniques: A Pure Sine Wave Inverter", Major Qualifying Project, Department of Electronics and Communication, Worcester Polytechnic Institute, Massachusetts, USA, 2011.

[9] Martina Calais, Lawrence J. Borle, and Vassilios G. Agelidis, "Analysis of Multicarrier PWM Methods for a Single Phase Five Level Inverter", *IEEE 32 Power Electronics Specialists Conf.*, pp. 1351-1356, 2001.

[10] Tengfei Wang, and Yongqiang Zhu, "Analysis and Comparison of Multicarrier PWM Schemes Applied in H-Bridge Cascaded Multi-level Inverters", *5th IEEE Conf. on Industrial Electronics and Applications*, pp. 1379-1383, 2010.

[11] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans on Industrial electronics*, vol. 49, no. 4, pp. 724–738, Aug,2002.

[12] Ned Mohan, Tore M. Undeland, and William P. Robbins, "Power Electronics, Converters, Applications and Design", Third Edition, New Delhi, Wiley India (P.) Ltd, Reprint 2007.M. H. Rashid, "Power Electronics: Circuits, devices and applications.