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Nine Level Inverter Using Modified H Bridge Configuration

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Abstract **The Inverter is an electrical device which converts direct current (DC) to alternate current (AC). The inverter is used for emergency backup power in a home. Inverters can be broadly classified into single level inverter and multilevel inverter. Generally multi-level inverters are preferred because it has been confirmed through experiments that, a multi-level inverter has reduced total harmonic distortion (THD) when compared to classic inverters and they can operate at several voltage levels. Also it has been inferred that, as the number of levels in the inverter increases, the distortion is further reduced. Thus, to have a better output, multi-level inverters of higher levels are used. Depending on the requirements, the number of levels is fixed for the inverter.The objective of this project is to develop a nine level inverter using modified H-Bridge configuration to drive a AC load. There are three configurations in multi-level inverters out of which, Cascaded H-bridge configuration is chosen to implement nine-level inverter.Nine-level inverter is used in place of standard inverters in order to get a close to sine wave output. A classic inverter has two output levels. One is +Vdc and another is –Vdc. A nine level inverter has nine levels in output waveform which are +4Vdc, +3Vdc, +2Vdc, +Vdc, 0, -Vdc, -2Vdc, -3Vdc, -4Vdc. A nine-level inverter is used in practice to supply motor drives, electrical vehicle drives, DC power source utilization, etc.**

Key Words: **Multi-level inverter, Total harmonic distortion, Cascaded H-bridge**

I. INTRODUCTION

Multilevel power converters have become popular in recent years due to the advantages of high power quality waveforms, less harmonic distortion, low common mode voltage, low switching operations, medium, high-voltage and high power capability. However, it increases the number of switching devices and other components, which results in an increase of complexity problems and system cost. Generally inverter is a device that converts DC electrical power to AC form using some electronic circuits. Simple inverter gives 2 or 3 level output voltage. Multilevel inverter gives 3 or more output voltage levels. It produces a stepped output voltage with reduced harmonic distortion when compared to a 2 level inverter.There are different types of multilevel inverter circuits involved. The first topology introduced was the series H-bridge design. Which was followed by the diode clamped converter, this utilized a bank of series capacitors. A later invention used the flying capacitor design in which the capacitors were floating rather than series-connected. Another multilevel design involves parallel connection of inverter phases through inter-phase reactors. In this design, the semiconductor blocks the entire dc voltage, but shares the load current. Several combinational designs have emerged, some involving cascading of the fundamental topologies. These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels. The multilevel inverters are mainly classified as diode clamped, flying capacitor inverter and cascaded multilevel inverter. The cascaded multilevel control method is very easy when compare to other multilevel inverter because it doesn't require any clamping diode and flying capacitor.It provides higher output voltage and power levels. It is one of the methods used for drive application which meetthe requirements such as high power rating with reduced THD and switching losses. In this paper, we are using a new topology by modifying the cascaded H-bridge multilevel inverter for producing nine output voltage levels using pulse width modulation technique.

II. PROPOSED SOLUTION

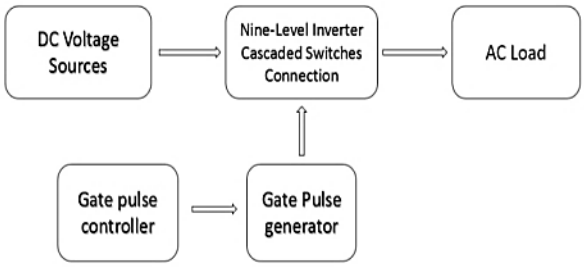

Figure 1: Simple Block Diagram of Nine levels Inverter

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The DC voltage is obtained by stepping down the single phase 230V AC voltage using a step down transformer and giving it to the rectifier circuit and obtaining a regulated DC voltage by using a DC voltage regulator. The Nine level cascaded switch connectionsare formed by cascading two modified 5 level Inverters. The switches need to be gate controlled which requires some technique to generate the gate pulses. Considering the required number of switches and other equipment required, modified H-bridge technique has been employed, which uses less number of switches and gate drives without compromising on the power loss and harmonic reduction. This nine level inverter is used to drive an AC load.

III. TECHNICAL ASPECTS OF SWITCHING DEVICE

Since it needs switches which operate depending on different time intervals, power electronics switches are used. Coming to the choice of switches, IGBT switches are preferred due their capacity to conduct with extremely less power loss and at very high switching frequencies. Also its voltage controlled property of gate terminal comes in handy while switching off the device. As to the choice of H-bridge, it is very simple and uses less number of components compared to diode clamped or flying capacitor type inverters.

3.1 Basic Switching Block Of A Modified H-Bridge Inverter

The main disadvantage of the conventional cascaded H-bridge is that when the voltage level increases, the number of semiconductor switches increases and also the source required increases. In order to overcome this new topology is introduced by modifying the cascaded H-bridge configuration. The main advantage of this topology is that the number of switches required is reduced. Figure 1 shows the five level inverter using modified H-bridge configuration. A cascaded five level inerter two three level inverter cascaded together, while the modified H Bridge is formed by cascading a three level inverter with an additional IGBT. Four diodes are connected to the IGBT in the left and are used to enable the switching device to conduct both from left to right and right to left. Though considered as one of the disadvantages, the use of many DC voltage sources becomes a necessity to control the levels of the output.

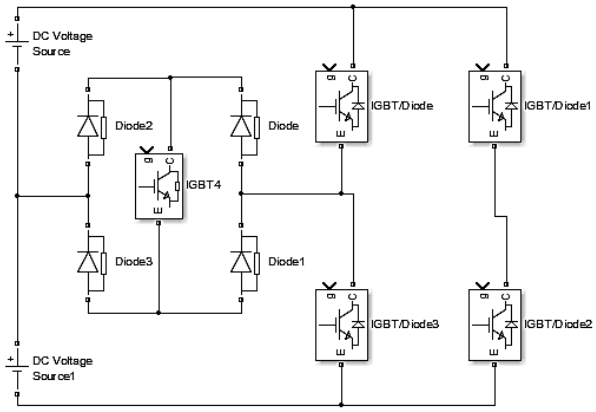

Figure 2: Five level inverter using modified H-bridge configuration

IV. CIRCUIT DIAGRAM FOR MODIFIED H-BRIDGE INVERTER

The nine-level modified H-bridge inverter was designed using SIMULINK software. The model is obtained from the modified H-bridge configuration for five level inverter. This provides an understanding of how theswitching processes can be controlled and how to reduce the switching changes, making it optimal.

This model of nine-level inverter requires ten switching devices connected in the manner shown in figure 3. Controlling the ON period of the switches and the firing angles, an output with nine-levels is obtained.

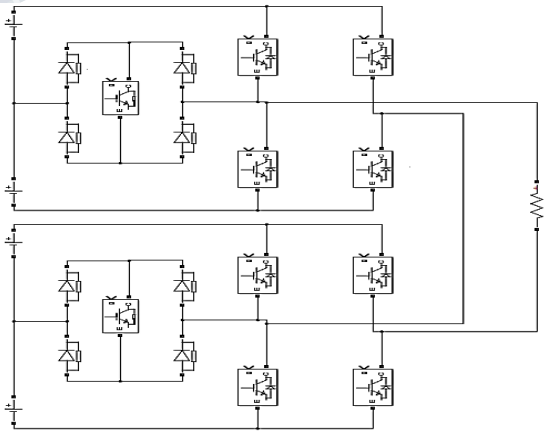

Figure 3: Nine level inverter using modified H Bridge configuration

As it can be seen from figure 3, the part containing five switches and two DC sources constitute the modified H-Bridge configuration of the five level inverter. Two of such combinations are cascaded and a nine-level inverter is obtained. The resistor on the right side of the circuit

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represents the load that has been used to study the behavior of the circuit.

Now the operation of the circuit is purely based on the firing angles chosen and the time for which the gate pulses of the IGBT switches are kept in the ON state. The figure 4 shows the naming of the switches which makes it convenient for toggles.

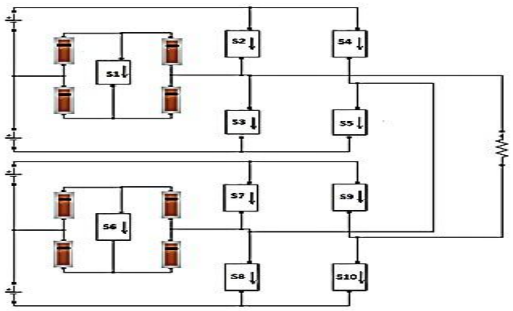

Figure 4: Simplified circuit diagram of Nine level inverter using modified H-Bridge configuration

The figure 4 shows the simplified circuit diagram for the ease of explaining the operation of the circuit. The diodes are represented in brown color; the black line represents the cathode side of the diode. The diodes are connected in such a way that it allows flow of current both from right to left and from left to right. The IGBT switches are represented in boxes with switch number,the arrow inside the boxes represents the direction of current flow through the anti-parallel diode present in the IGBT. The DC voltage sources are represented as they are and each DC source provides a voltage of V across them.

V. GENERATION OF TRIGGERING PULSES FOR IGBT'S BY USING LOGIC GATES

The gate pulses other than that of S1 and S6 are continuous over a particular time and repeat themselves in cycles of period 20ms. These pulses are easy to generate, while the pulses for S1 and S6 require additional attributes.
The pulses for S2, S3, S4, S5, S7, S8, S9, and S10 are generated by taking a 50% PWM pulse and performing logical AND operation with a normal PWM pulse. The trigger pulse for S5 and S10, S4 and S9 are the same. The 180 degree phase shifted pulses of S1, S2, S3, S5 are the trigger pulses for S6, S8, S7, S4 respectively.

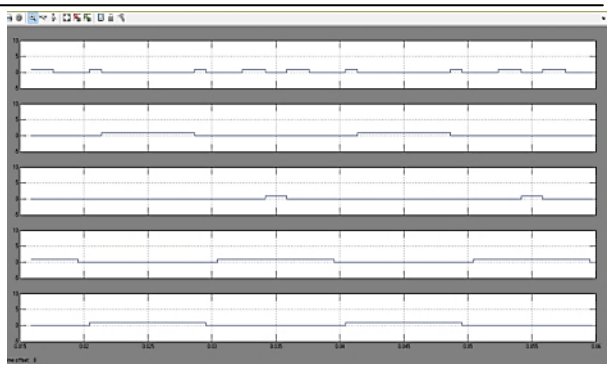

Figure 9: Triggering pulse for IGBT's S1 to S5

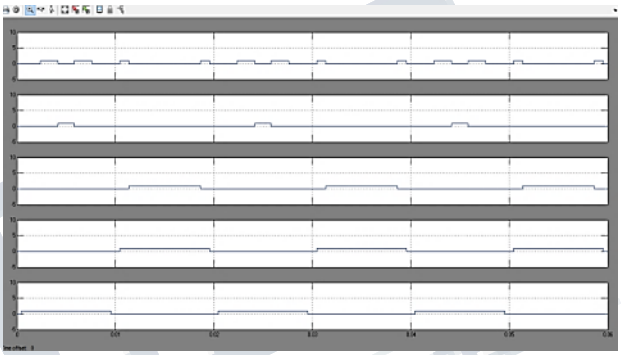

Figure 10: Triggering pulse for IGBT's S6 to S10

5.1 *Generation Of Gate Pulse Of S1 (Positive Half Cycle):*

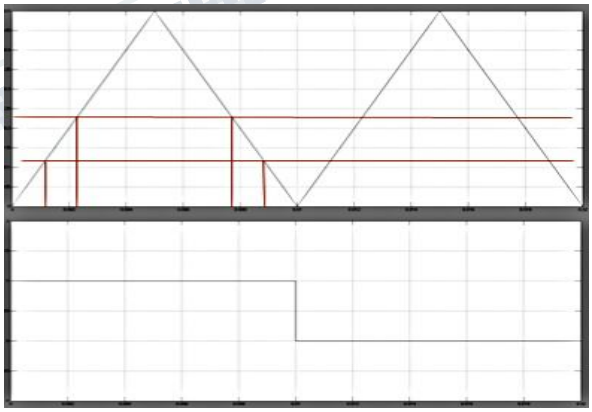

Figure 11: Triggering pulse generation for S1 (+ve half cycle)

To generate positive half cycle pulse for IGBT S1, a repeating triangle wave sequence is taken as shown in figure 11(top).The DC limits (horizontal lines) b, c are chosen based on the firing angle required.The high level is obtained when a crosses b but is within c (i.e., a-b > 0 and a-c < 0). Here, 'a' is used to represent the triangular pulse.This occurs for both the half cycles. To take the pulse only for the positive half-cycle, the output is logically AND with the signal shown in figure 11(bottom).This makes the pulse available only in the positive half cycle.

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5.2 ***Generation Of Gate Pulse Of S1 (Negative Half Cycle):***

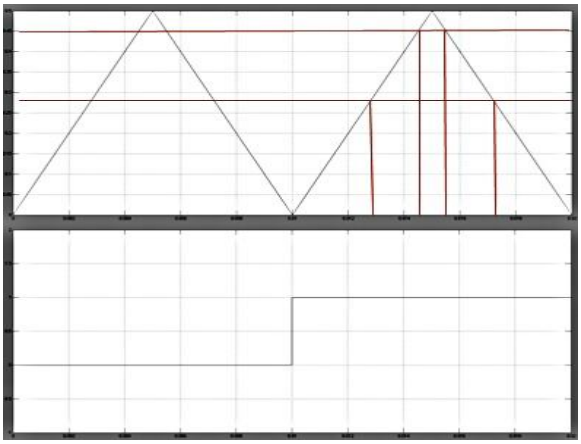


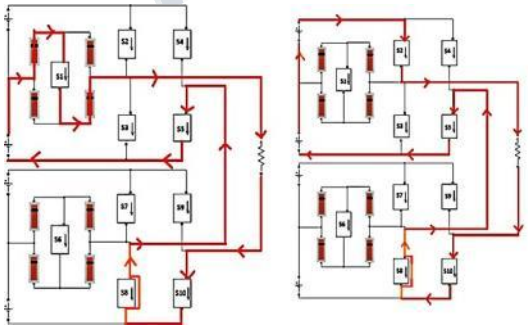
Figure 12: Triggering pulse generation for S1 (-ve half cycle)

To generate negative half cycle pulse for IGBT S1, a repeating triangle wave sequence is taken, as shown in figure 12(top). The DC limits (horizontal lines) b, c is chosen based on the firing angle required. Similar to the sampling in positive Half cycle, the high level is obtained when a crosses b but is within c (i.e., a-b > 0 and a-c < 0). This occurs for both the half cycles. To take the pulse only for the negative half-cycle, the output is logically AND with the signal shown in figure 12(bottom). This makes the pulse available only in the negative half cycle.

VI. CIRCUIT OPERATION

The firing angles of the switches are chosen such that a reduced total harmonic distortion is obtained. Based on the calculations for a THD of 12.31% by distortion minimization PWM technique, the value of $\alpha 1$ is 8.2147, α_2 is 25.128, α_3 is 45.417, and α_4 is 87.5979.

The figure 5 shows the switching of different IGBTs in the circuit and the corresponding current flow in the branches of the circuit during the positive half cycle of the output waveform.



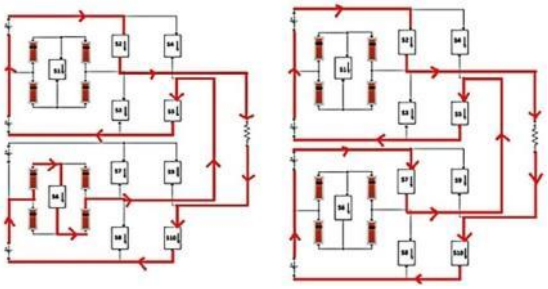


Figure 5: Switching operations and current flow for positive half cycle of output voltage.

The figure 6 shows the switching of different IGBTs in the circuit and the corresponding current flow in the branches of the circuit during the negative half cycle of the output waveform. It can be seen that the direction of current flow through the load is reversed as a result of reverse bias across the load

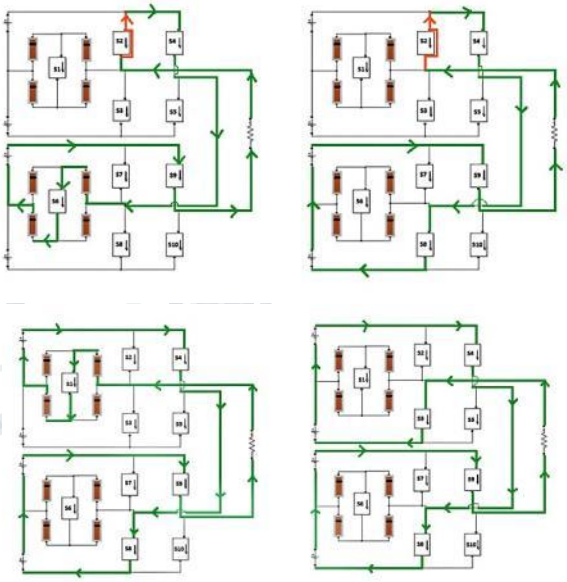


Figure 6: Switching operations and current flow for negative half cycle of output voltage.

The flow of current is shown with a different color at some places in both positive and negative half cycle represent that the current flows through the antiparallel diode connected across every IGBT which can be seen in the circuit diagram. These diodes also provide freewheel path for current during switching off of the IGBT which will help reduce the effect of Miller Capacitance.

VII. RESULTS AND DISCUSSIONS:

The figure 7 and figure 8 represents the output voltage and output current for one full cycle respectively.

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The Switching operations in order to get a close to sine wave output are consolidated and given in table1.

By using a modified H-Bridge configuration the number of switching devices and gate drivers are greatly reduced and a close to sine wave output with less total harmonic distortion is obtained.

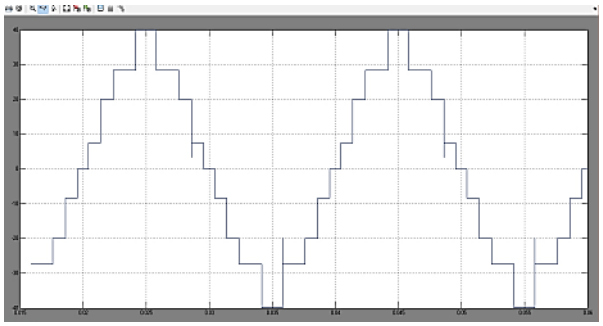

Figure 7: Output voltage for one full cycle

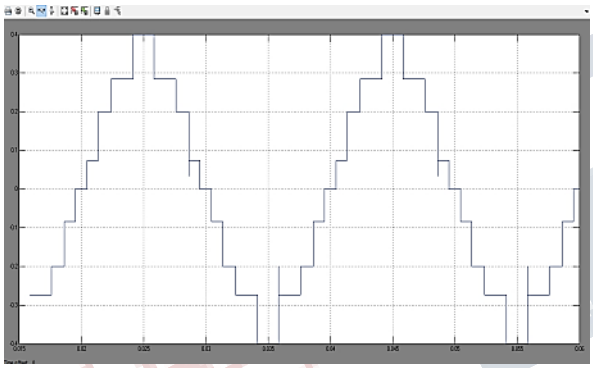

Figure 8: Output current for one full cycle

	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
0V										
1V	•				•					•
2V		•			•					•
3V		•			•	•				•
4V		•			•		•			•
4V		•			•		•			•
3V		•			•	•				•
2V		•			•					•
1V	•				•					•
0V										
-1V				•		•			•	
-2V				•				•	•	
-3V	•			•				•	•	
-4V			•	•				•	•	
-4V			•	•				•	•	
-3V	•			•				•	•	
-2V				•				•	•	
-1V				•		•			•	
0V										

Table1: Switching of various IGBT's

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