

Studies on PWM Inverter Employing Series-Connected Capacitors Paralleled to a Single DC Voltage Source

^[1]Rashmi D S, ^[2]Pradipkumar Dixit

^[1] M.Tech Student, ^[2] Professor,

Dept. of Electrical and Electronics Engineering
M.S Ramaiah Institute of Technology, Bangalore, India

Abstract: - This paper presents an effective circuit configuration of a multilevel inverter of single DC independent voltage source that can increase the number of output voltage levels with a less number of circuit components. To produce the output voltage levels the Seven-level pulse width modulation inverter consists of a single dc voltage source with a series of three capacitors, two diodes, three active switches and H-bridge cell. Here using modified switching strategy to solve the voltage unbalancing that occurred in series connected capacitors and THDv. MATLAB/Simulink software is used in the simulation and results are compared with the published data.

Keywords—multilevel inverter, single DC sources, PWM, H-Bridge, Voltage unbalancing, THDv.

I. INTRODUCTION

Nowaday's multilevel inverter (MLI) are more popular because of medium and high power applications in industries. Multilevel inverter generates output voltage in staircase waveforms with reduced harmonic distortion. Among the well-known various types of topology, Cascaded H-bridge (CHB) were convenient to use in industrial applications (fans, pumps, compressor etc.) due to less number of power electronics component and reduced voltage stress across switches. Output voltages of CHB obtained by summing positive, zero and negative voltage levels [1]. PWM inverter converts DC to AC with variable frequency that can feed to ASD's for variable speed and variable frequency applications. Main objective is to produce the voltage waveform close to sinusoidal with offering some filter of lower size capacitance to reduce the distortion in the output voltage [1].

MLI is used to synthesize the output voltage near to sinusoidal from several levels. As the voltage level increases waveform becomes smoother, along with that power electronics components and complexity of circuit increases. With the increase of number of levels, THD decreases. . It is clear that an output voltage with low THD is desirable, but it increases the number of levels requires more hardware and also the control will be more difficult. It is a substitution between price, complexity, weight, and a

very high-quality output voltage with less THD and minimum voltage source [2].

II. SEVEN-LEVEL PWM INVERTER USING R-LOAD

2.1 Seven-Level PWM Inverter of Single Dc Source Using R-Load

A. Circuit Configuration

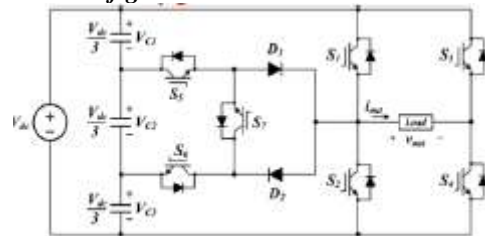


Fig.2.1 Circuit diagram of seven level PWM inverter of single DC source

Figure. 2.1 shows a circuit arrangement of the used seven level PWM inverter. It has a voltage source of single DC, which is separated by three capacitors joined in series. Let us suppose that all components are ideal and that the circuit is in a steady state. Voltage of each capacitor is equal to $V_{dc}/3$. Then, we can attain seven levels in the output voltage, i.e., V_{dc} , $2V_{dc}/3$, $V_{dc}/3$, 0 , $-V_{dc}/3$, $-2V_{dc}/3$, and $-V_{dc}$. The switches in an H-bridge cell (S1~S4) work to resolve the polarity of the output

voltage with the highest (or lowest) voltage level, i.e., V_{dc} (or $-V_{dc}$). Other voltage levels are produced by S_5 , S_6 , and S_7 .

B. Generation of Output Voltage Levels

Positive Two Level: When source voltage is given, capacitors are charged. This capacitor starts discharging and acts as source as well as filtering circuit. When Switch S_1 and S_4 are turned ON, current flows through the load is positive. Hence positive voltage appears and waveform starts from positive cycle as shown in Fig.2.1. (a).

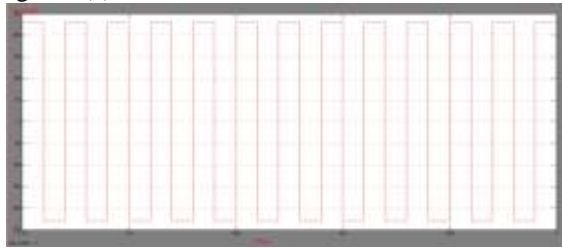


Fig.2.1.(a) Positive Two Level voltage

Negative Two Level: When Switch S_3 and S_2 are turned ON, current flows through the load is negative. Hence negative voltage appears and waveform starts from negative cycle as shown in Fig.2.1. (b).



Fig.2.1.(b) Negative Two Level voltage

Positive Level: When Switch S_5 is turned ON, will get two level positive voltage, similarly when S_6 and S_7 are turned ON, will get another two level positive level and when S_5 , S_6 and S_7 are turned ON, will get positive voltage of two and three level Fig. 2.1. (c).

Three Level: When Switch S_1 and S_4 are turned ON, will get positive voltage level, similarly when S_3 and S_2 are turned ON, will get negative voltage level and when both S_2 and S_4 are turned ON, will get zero voltage level. When all switches are turned ON, i.e., under continuous conduction mode will get positive zero and negative voltage i.e., three level output voltage Fig. 2.1. (d).



Fig. 2.1.(c) Positive Level

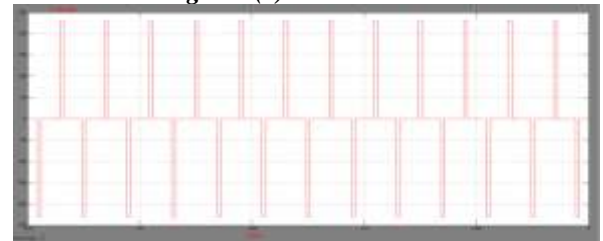


Fig. 2.1.(d) Three Level voltage

Five Level: When Cascaded H-Bridge is turned ON, will get three level output voltage and when S_5 and S_6 are turned ON, will get positive two level output voltage. Combining three and two output voltage will get a five level output voltage Fig. 2.1. (e).

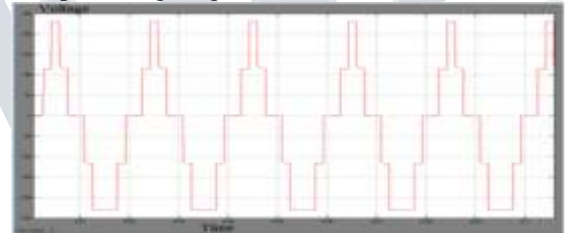


Fig. 2.1.(e) Five Level voltage

Seven Levels: When Cascaded H-Bridge is turned ON, will get three level output voltage and when S_5 , S_6 and S_7 are turned ON, will get positive two and three level output voltage. Combining three and two output voltage will get an Seven level output voltage Fig. 2.1. (f).

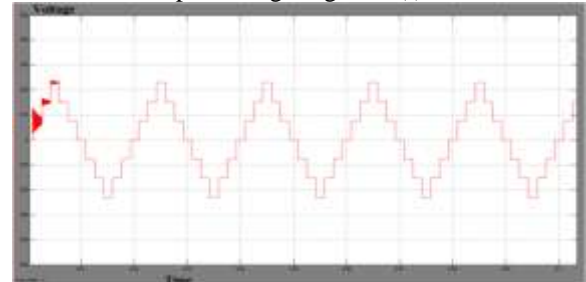


Fig. 2.1. (f) Seven Level voltage

C. THDv Analysis

To know the percentage value of total harmonic distortion (THD) of the output voltage waveform FFT analysis is done. Figure. 2.1.(g) shows the fast Fourier analysis of seven level inverter of single DC source. For the purely resistive load THD value is 7.24.

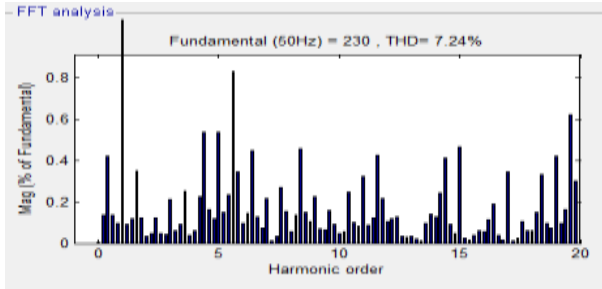


Fig.2.1. (g) FFT Analysis of Seven Level voltage

D. Capacitor Voltage Balancing

For the multilevel inverter output voltage greater than three levels does not require separate DC voltage source. By proper control and support capacitors can replace the separate DC voltage source. To control and maintain each voltage level they require either voltage balancing circuit or single DC sources for the active power transfer applications.

Voltage imbalance and voltage fluctuations occurred on the floating capacitors by using a control method to stable the voltage for an average value. In order to suppress the fluctuations of voltage by injecting a high frequency voltage of zero sequence and circulating current is used, that can be used for the starting of induction.

If a string of capacitors are connected in series, then the same charge flows as the same current flows in a given time. When a H-Bridge cell is turned on, current flows through each capacitor. The capacitor charges and discharges, this causes fluctuation in the capacitor voltage. This happens because due to different switching ON and OFF time, unequal conduction, switching loss of the device and unequal active power units of H-Bridge. This causes imbalance in the voltage distribution across the each capacitor arm.

By maintaining the capacitor voltage constant, desired voltage levels can be achieved. To attain equal voltage levels, each arm can be made equal to the average value of reference voltage. For that capacitor is set to have a specific value for initial voltage which is equal to $V_{dc}/3$ voltage level. This value of capacitor is compared with the actual voltages. Hence capacitor balances the internal voltage.

Here each capacitor value is nearly equal to the reference value of voltage i.e., $V_{dc}/3$ voltage level. Fig 2.1.(h) shows the voltage balancing of capacitors by referring some initial value of voltage. Capacitor C1 starts with positive level as current flows is positive and similarly capacitor C3 starts with negative level as current flows is negative. Middle capacitor C2 maintains the reference voltage $V_{dc}/3$ (76 V) and other capacitors C1 and C3 support $V_{dc}/3$ (79 V) with some ripples affected by an input voltage source.

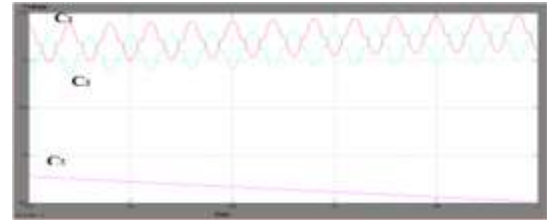


Fig.2.1.(h). Simulation results with the modified switching method. Balanced voltage in series-connected capacitors.

2.2 Seven-Level Inverter Of Separate Dc Source Using R-Load

A. Circuit Configuration

Single level generates positive, zero and negative voltage levels. Using dissimilar combination of switches, voltage levels can be obtained. Many H-Bridge inverters are connected in series to get sinusoidal output voltage [5]-[8]. Actually the output voltage generated is the sum of each cell. If there are n cells then number of output voltage levels will be $2n+1$. As the number of cells increases output voltage level increases for several levels it reaches nearly too sinusoidal. For Example single H-Bridge inverter generates three level output voltage, two H-Bridge inverter generates five levels, three H-Bridge inverter generates seven levels Fig.2.2.1.

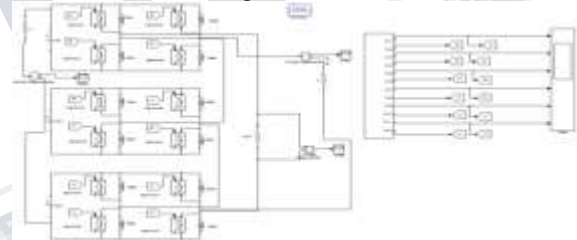


Fig.2.2 Model of seven level PWM inverter of separate DC source

B. Generation of Output Voltage Levels

Three Level(3L): When source voltage is given switch S1 and S4 are turned ON, will get positive voltage level, similarly when S3 and S2 are turned ON, will get negative voltage level and when both S2 and S4 are turned ON, will get zero voltage level. When all switches are turned ON, i.e., under continuous conduction mode will get positive, zero and negative voltage i.e., three level output voltage Fig.2.2.(a).

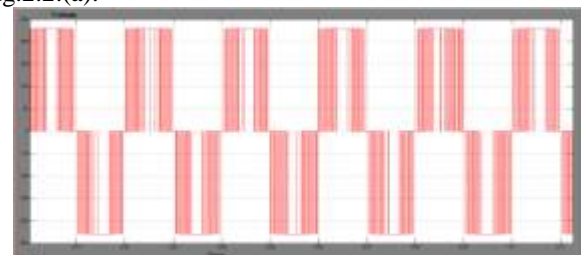


Fig.2.2.(a) Three Level voltage

Five Level(5L): Cascading another one H-Bridge cell in series increase the output voltage level from three to five level Fig.2.2.(b).

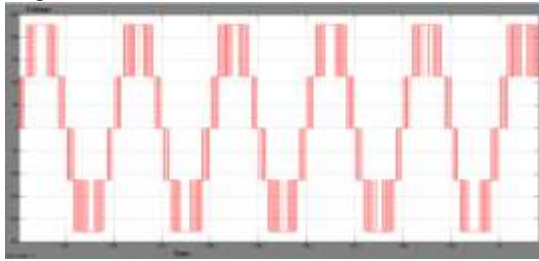


Fig.2.2.(b) Five Level voltage

Seven Level(7L): Cascading two H-Bridge cell in series gives five level and similarly cascading three H-Bridge cell in series gives seven level Fig.2.2.(c).

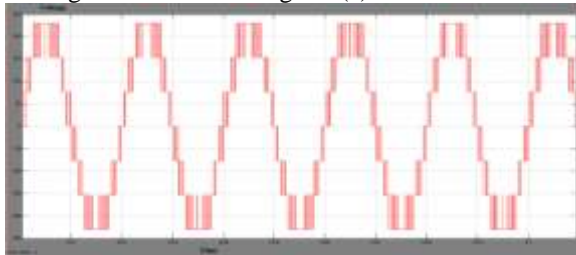


Fig.2.2.(c) Seven Level voltage

C. THDv Analysis

As there is increase in number of cascaded H-Bridge cell, output voltage levels also increases with reduction in the THDv.

Table.1 comparing various parameters THDv of three, five and seven level separate DC source

PARAMETERS	SEPERATE DC VOLTAGE SOURCE (3L)	SEPERATE DC VOLTAGE SOURCE (5L)	SEPERATE DC VOLTAGE SOURCE (7L)
Input Voltage	230V	230V	230V
R Load	50Ω	50Ω	50Ω
Input Current	4.6A	4.6A	4.6A
Diodes	12	2	2
Switches	12	3	3
Capacitor	-	3	3
Output Voltage	230V	230V	230V
Output Current	4.6A	4.6A	4.6A
Frequency	50Hz	50Hz	50Hz
THDv	18.70%	10.59%	9.90%

Table.2 comparing various parameters of seven level separate and single DC source

PARAMETERS	SEPERATE DC VOLTAGE SOURCE	SINGLE DC VOLTAGE SOURCE
Input Voltage	230V	230V
R Load	50Ω	50Ω
Input Current	4.6A	4.6A
Diodes	12	2
Switches	12	3
Capacitor	-	3
Output Voltage	230V	230V
Output Current	4.6A	4.6A
Frequency	50Hz	50Hz
THDv	9.90%	7.24%

Comparing the various parameters of separate and single DC sources, we can conclude that single DC source uses

less number of diodes, switches and even there is a decrease in the THD value. So it is better to use a power electronic circuit with good reduction in THD value as well voltage sources as economy cost is concerned and reduction in the hazardous effect which further increase in the life of the electrical drives system [9].

III. SIMULATION RESULTS AND DISCUSSIONS

A. IMPLEMENTING SEVEN-LEVEL INVERTER OF SINGLE DC SOURCE USING INDUCTION MOTOR

Here simulation is done for single and separate DC sources and speed is verified by keep the motor torque value of 0.5 N-m, and speed waveform are shown in the following.

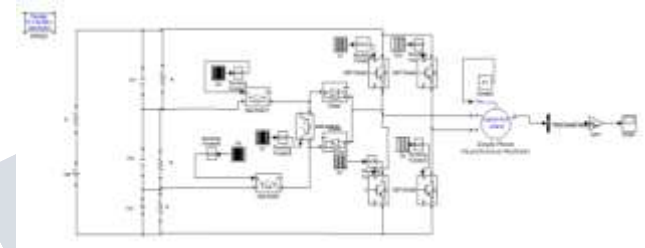


Fig.3.1 Model of Seven level single DC source using capacitor start IM

Figure.3.1 shows the MATLAB simulation of capacitor start IM using Single DC source. Figure.3.2 shows speed waveform of capacitor start IM using Single DC source. Here stator the speed is almost nearer to synchronous rotor speed. Since the distortion is less in the output voltage.



Fig.3.2 Speed of Seven level single DC source using capacitor start IM

B. Implementing seven-level inverter of separate dc source using induction motor

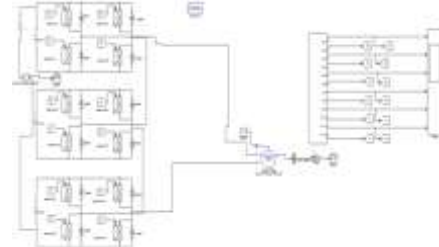


Fig.3.3 Model of Seven level separate DC source using capacitor start IM

Figure.3.3 shows the MATLAB simulation of capacitor start IM using separate DC source. Figure.3.4 Speed waveform of capacitor start IM using separate DC source. The stator the speed is varied to synchronous rotor speed. Since the distortion is more in the output voltage.

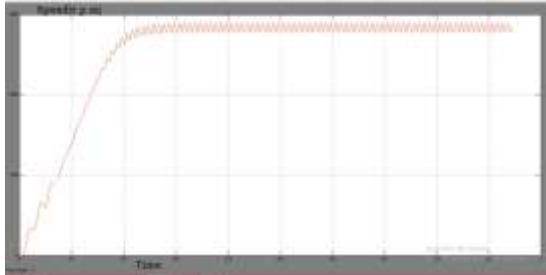


Fig.3.4 Speed of Seven level separate DC source using capacitor start IM

C. Discussions

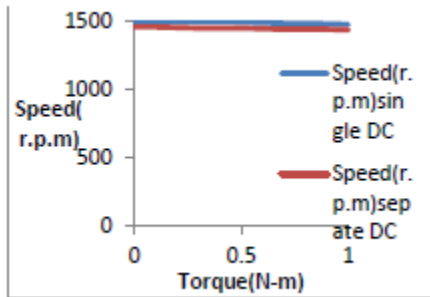


Fig.4.1 Graph shows torque v/s speed curve

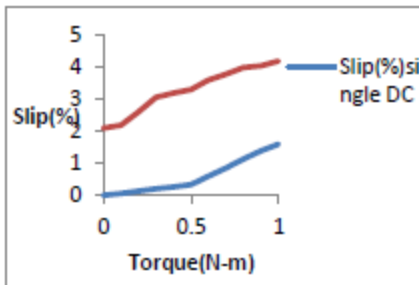


Fig.4.2 Graph shows torque v/s slip curve

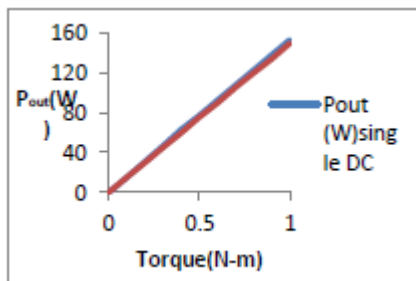


Fig.4.3 Graph shows torque v/s output power curve

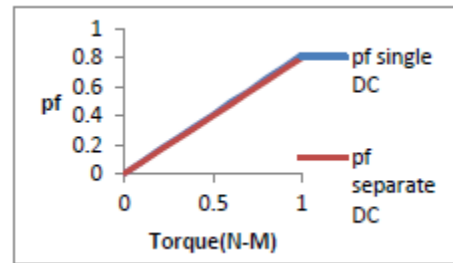


Fig.4.4 Graph shows torque v/s power factor curve

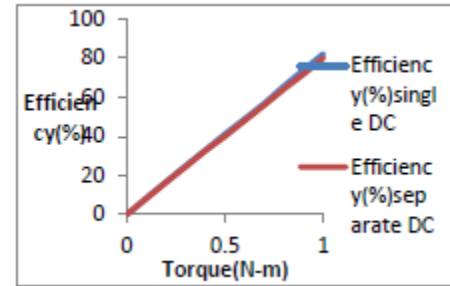


Fig.4.5 Graph shows torque v/s efficiency curve

Figure.4.1 Graph shows torque v/s speed curve, as torque varies speed also varies; single DC reaches maximum speed compared to separate DC. Figure.4.2 Graph shows torque v/s slip curve, as speed reaches maximum value, percentage of slip is less in single DC. Figure.4.3 Graph shows torque v/s output power curve, output power drawn is more in single DC source. Figure.4.4 Graph shows torque v/s power factor curve, power factor is improved in single DC source. Figure.4.5 Graph shows torque v/s efficiency curve, efficiency of the motor is better in single DC source. From the graphs we can conclude that Single DC source gives better performance in various parameters.

V. CONCLUSION

The paper discusses the implementation of cascaded H-Bridge multilevel inverter (CHBMLI) with low total harmonic distortion for the improvement of performance of motor load. Various inverter topologies have been compared based on required number of switching devices, capacitors, etc, for same level of inverter and finally CHBMLI topology has been found to be perfect choice for high voltage and power applications. Using the MATLAB Simulink software CHBMLI fed induction motor is simulated and the results were obtained as expected.

REFERENCE

- [1] I.Colak, E.Kabalsi, "Practical implementation of a digital signal processor controlled multilevel inverter with low total harmonic distortion for motor drive applications", ELSEVIER, Journal of Power Sources 196 (2011) pp.7585–7593.
- [2] J.Rodriguez, Senior Member IEEE, Leopoldo G. Franquelo, Fellow IEEE, Samir Kouro, Member IEEE, Jose I. Leon, Member IEEE, "Multilevel Converters An Enabling Technology for High-Power Applications", IEEE Vol. 97, No. 11, Nov.2009.
- [3] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," in Conf. Rec. IEEE IAS Annu. Meeting, 2000, pp. 2024–2031.
- [4] Jin-Sung Choi and Feel-soon Kang, "Seven-Level PWM Inverter Employing Series-Connected Capacitors Paralleled to a Single DC Voltage Source", IEEE Trans. Ind. Electron., vol. 62, No. 6, June 2015, pp. 3448-3459.
- [5] V.K. Chinnaiyan, J. Jerome, J. Karpagam, T. Suresh, "Control techniques for Voltage Source Inverters", IEEE IPEC'07 (2007) pp.1023–1028.
- [6] K.Gopakumar, Mariusz Malinowski, Jose Rodriguez, and Marcelo A. Pérez, "A Survey on Cascaded Multilevel Inverters", IEEE Trans on Industrial Electronics, vol. 57, no. 7, July 2010.
- [7] K.A.Corzine, M.W.Wielebski, F.Z.Peng, J. Wang, "Control of cascaded Multilevel Inverters", IEEE Trans. Power Electron.19 (2004) pp.732–738.
- [8] Roozbeh Naderi and Abdolreza Rahmati, "Phase-Shifted Carrier PWM Technique for General Cascaded Inverters," IEEE Trans on power Electronics, vol. 23, no. 3, May 2008.
- [9] B.P. McGrath, D.G. Holmes, and T. Meynard, "Reduced PWM harmonic distortion for multilevel inverters operating over a wide modulation range," IEEE Trans. Power Electron., vol. 21, no. 4, pp. 941–949, July 2006.