

# High Frequency Boost Converter

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**Abstract:** - Converter based on two switching cells is proposed. These switching cells are connected in parallel so the average current flowing through the switch is reduced by the duty cycle. The different relevant characteristics of the proposed circuit are, the controlled switches having drop voltage across them is low, that permits the use of lower drain-to-source conductivity resistances (RDSon) MOSFETs, and magnetic components size is reduced due to the high operating frequency. Hence the scale and volume of the converter is reduced. Due this approach, the efficiency of the projected device is high, and it is suggested for the space application. This device is analysed for the load from 16.66% to full load operative in continuous conduction mode (CCM) and with maximum duty cycle of 48%. So as to verify the practicability of this topology; operation of the device, theoretical examination, and exploratory waveforms are shown for a 300W assembled prototype.

**Index Terms**—continuous current mode, discontinuous current mode, EMI filter

## I. INTRODUCTION

AS so much as satellite are considered, the obtainable performances are inevitably restricted by the capacity of the launcher and a powerful effort is formed to convert any mass saving into further payload capability[1]. A continuing analysis is applied on each sub-system of the space vehicle platform and payload so as to scale back their mass and build their operation a lot of economical. Hence the benefits of technique include higher efficiency at high switching frequencies and lower component stresses.

Assuming that ability will be increased, whereas increasing the operational frequency, proportionately lower values of energy storage components yield size reduced converter as well as less weight power converter. Modern electronics systems need the high-quality, small-size, light-weight, reliable, and economical power supplies. Linear power regulators are restricted to output power smaller than the input power and additionally power density is less as a result of they need low frequency (50 or 60 Hz) line transformers and filters. Linear regulator is confined to produce only a lower controlled output from higher unregulated input. Regulation ability of linear regulator is low, resulting power loss. To overcome this limitation of linear regulator, switch mode power supplies are used as alternative in most of modern electronics applications. Switching regulators use semiconductor switch which produces the unregulated DC-input voltage to a controlled output voltage. The square shape wave with adaptable duty cycle is enforced to output low pass filter to obtain

controlled DC output[2]. They generate buck, boost and inverted outputs. Isolated and non-isolated converters are two types of switch mode power supplies among which buck, boost and buck-boost are non-isolated converters, whereas flyback, push-pull, full-bridge and half bridge are isolated converters. For applications requiring high power outputs isolated converters can be employed. Designing of boost converter with high operating frequency having remarkable applications such as, High switching devices such as MOSFET/IGBT is used as switching device with high switching frequency, due to which switching losses are reduced. Due to this high operating frequency right half plane zero effect is reduced from this high bandwidth can be achieved.

The basic operation of boost converter will now be explained. Figure1 shows the boost regulator power stage and figure2 the simplified waveform of voltage and current.

## II. BOOST CONVERTER

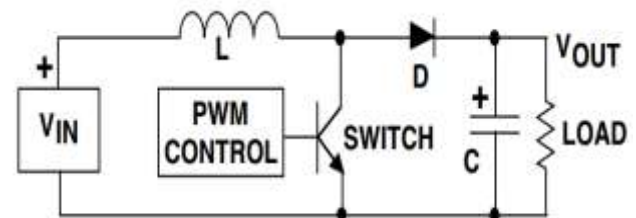
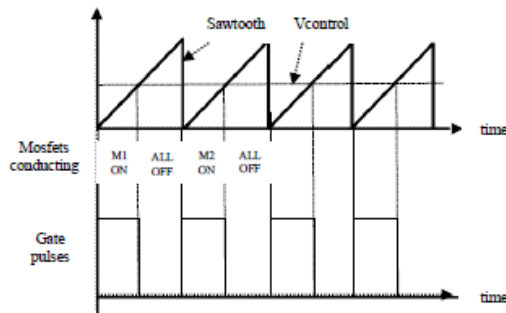


Fig. 1: (a) Boost converter

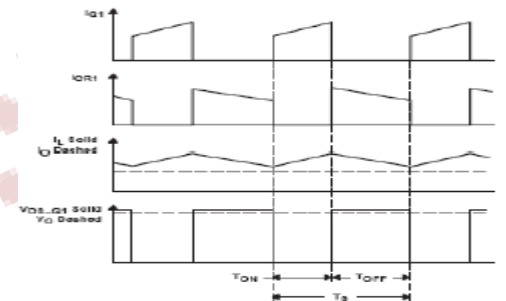
The switching topography used for the boost converter is that the bipolar switching of voltages, where the MOSFET's are switching in complementary form.

Each switch will conduct for 125KHz switching frequency so the effective switching frequency will be 250KHz. The basic diagram of boost converter is shown within the fig 1(a).

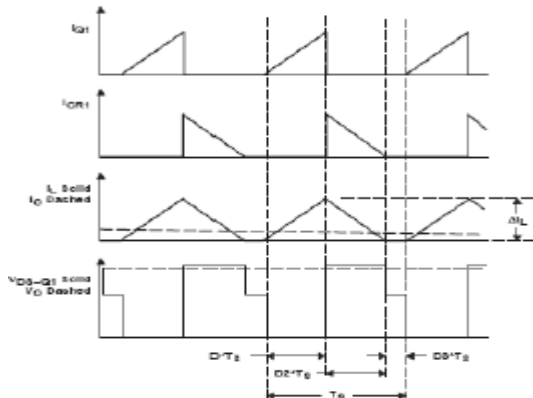
The voltage at the output  $V_o$  is controlled and adjusted by the Pulse Width Modulation approach seen in fig. 1(b) wherever a saw tooth signal is in comparison with a voltage control signal from the feedback loop. Throughout the primary period, the switch M1 is ON as long because the saw tooth signal is not up to the control signal. Once it exceeds the control level the switch will be OFF till the second half cycle takes place when the switch M2 starts to conduct till the saw tooth signal once more exceeds the control level, these steps repeats throughout the cycle



**Fig. 1: (b) Boost converter switch topology**



**Fig. 1: (c) Continuous current mode**



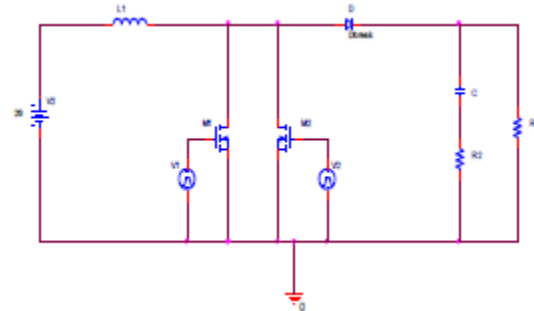
**Fig. 1: (d) Discontinuous current mode**

Fig 1(c) and 1(d) shows the continuous current mode and discontinuous mode of the converter, where  $I_{Q1}$  is the MOSFET current waveform,  $I_{CR1}$  is the diode current waveform,  $I_L$ (solid ) inductor current waveform,  $V_{DS}$  is the voltage across MOSFET when it is in OFF condition. An important construction of the boost regulator is that the load current and the MOSFET currents are not equal and the most accessible load current is often but this current rating of the switch is high. It ought to be noted that most total power accessible for the conversion in any regulator is equal to the input voltage increased times the average input current (which is a smaller amount than this rating of the switch). Since the output power of boost is higher than the input power. It follows that the output current should be less than the input current.

**Input Filter**

The input filter on a switch power offer has 2 primary functions. First, is to stop electromagnetic interference, generated by the switch supply from reaching the power line and arming the other instrumentation. Second, the requirement of the input filter is to avoid the high frequency voltage on the power source line flowing through the output of the power supply. A passive L-C filter answer has the characteristic to realize each filtering necessities. The goal for the input filter architecture ought to be to realize the most effective compromise between realization of the filter with volume and price [3].

**III. CIRCUIT DIAGRAM AND DESCRIPTION**



**Fig. 2: Circuit diagram of proposed boost converter**

Above figure shows the schematic of a boost converter. It contains two active switches M1 & M2, with an inductor L, diode D and an output capacitor C. The duty cycle of an active switch is 48%. Pulse width modulation (PWM) technique has been adopted. That is, the gate signals of M1 and M2 are complementary. Delay times avoiding the co-occurring conduction of the switches. When M1 & M2 are conducts the inductor current divides equally and flows through the MOSFETs, due to this reduced current flow power dissipating across the switches also reduces.

In continuous current mode of boost converter, once the switch M1 is conducting, hold on energy builds with in the inductor L. Once the switch M1 is not conducting, energy transfer to the load side via diode D. The switch current could be a stepped saw tooth with a fixed ON time duration with some quantity of ripple current superimposed. During the conducting time of the MOSFET, if we tend to assume zero losses for the instant, the voltage across the inductor is close to the input voltage. During the ON time, the peak-to-peak inductor current is given as[4],

$$\Delta I_L(\text{ON}) = V_{IN}/L$$

Once the switch is not conducting, the energy hold on in the inductance transferred to the output via the rectifier. The voltage of the inductor is nearly the input-to-output voltage difference, and also the voltage of the switch is nearly the load voltage.

When switch is OFF, the peak-to-peak inductor current is given as,

$$\Delta I_L(\text{OFF}) = (V_{IN} - V_{OUT})/L$$

Switch conducting time is equated with the not conducting time of the switch over a period.

$$(V_{IN}/L) \times D \times T_s = [(V_{IN} - V_{OUT})/L] \times (1-D) \times T_s$$

$T_s$

Solving above equation, D, results as

$$DCCM \text{ (ideal)} = 1 - (V_{IN}/V_{OUT})$$

#### A. Specification:

1. Input specification:

VIN NOMINAL = 28

VIN MIN = 26V,

VIN MAX = 33V

EMERGENCY OPERATION: DC STEADY STATE VOLTAGE SHALL BE BETWEEN 26-33 V AND IS TAKEN CARE BY DESIGN.

#### 2. Output specifications

Vo = 50V

Io = 6A

3. Dmax limited to 0.48

4. Dmin = 0.34

5. Efficiency = 90%

6. Switching frequency, fs = 250KHz

7. Ripple voltage = 500mVp-p(max)

8. Output power = 300W

9. Input power = 333.33W

#### B. EMI FILTER designing:

Fundamental peak current from simulation is =1.33A

$$\text{RMS current} = \frac{1.33}{\sqrt{2}} = .93A$$

The limit level according to MIL – STD 461E, which is found to be 66.5 dBμV

$$66.5 \text{ dB}\mu\text{A} = 20 \log(V_{in}/1\mu\text{V})$$

$$V_{in} = 2.11 \text{ mV}$$

$$I_{in} = (2.11 \text{ V}/50 \Omega)$$

$$I_{in} = 42.26 \mu\text{A}$$

The required attenuation is calculated as = 1 milstd 461/

I fund , rms

$$1/(1 + (\frac{X_L}{X_C})) \leq \frac{42.26 \mu}{0.96}$$

$$= 4.402 \times 10^{-5}$$

Required attenuation = 86.85 dB @ 250 KHz

Impedance ratio of

$$\frac{1}{1 + (\frac{X_L}{X_C})} = 4.402 \times 10^{-5}$$

$$\frac{X_L}{X_C} = 22715.5$$

$$\frac{2\pi f L}{\frac{1}{2\pi f C}} = 1857$$

$$f_c = f_s \times 10^{\frac{06.05}{40}}$$

$$= 1685.35 \text{ Hz}$$

$$f_c = \frac{1}{2 \times \pi \times \text{sqrt}(L1 \times C1)}$$

$$LC = 4.7 \times 10^{-9}$$

To get the required attenuation, L1=110.7μH and C1 = 82 μF, is calculated. Here magnetic component inductance value is decreased due to the high switching frequency. The filter used is single stage differential mode filter.

To damp the peak value, a series combination of resistor and capacitor is connected across the filter.

$$C_{\text{damp}} = 4C_1$$

$$= 4 \times 82 \mu\text{F}$$

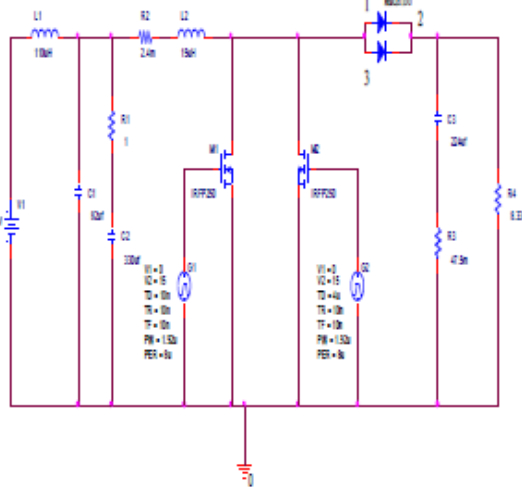
$$C_{\text{damp}} = 328 \mu\text{F}$$

$$R = \sqrt{\frac{L}{C}} = 1.16 \Omega$$

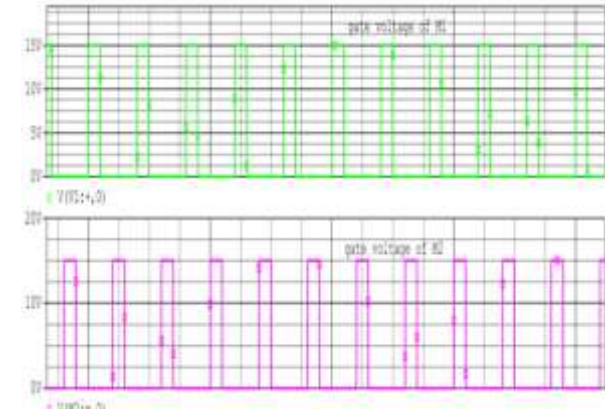
Damping components C3= 330uF, R= 1 Ω

**IV. SIMULATION CIRCUIT AND WAVEFORMS:**

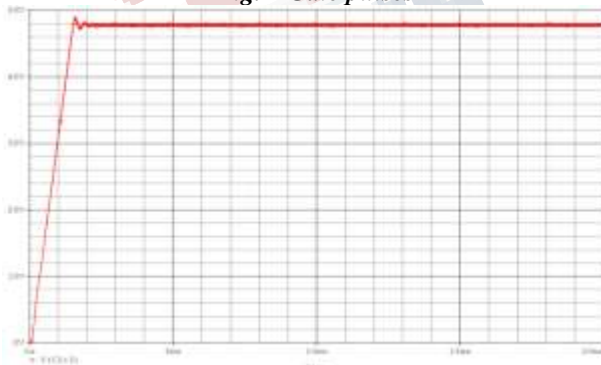
The proposed converter is designed and simulated using ORCAD software. The simulated results are given below. The proposed converter is shown in fig



**Fig. 3 Schematic of Proposed Boost Converter**

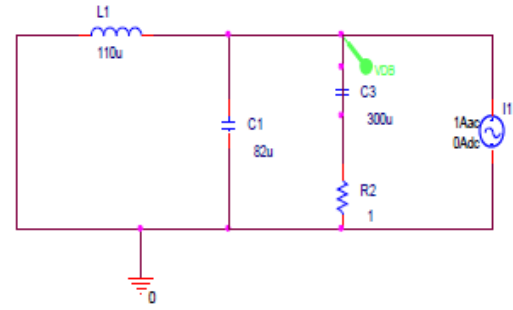


**Fig. 4 Gate pulses**

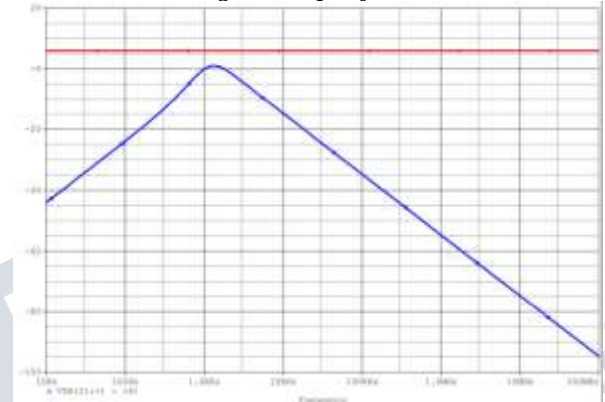


**Fig. 5 Output voltage**

The above graph are simulated results of proposed converter and fig 4 & 5 gives gate pulses and output voltage waveform.



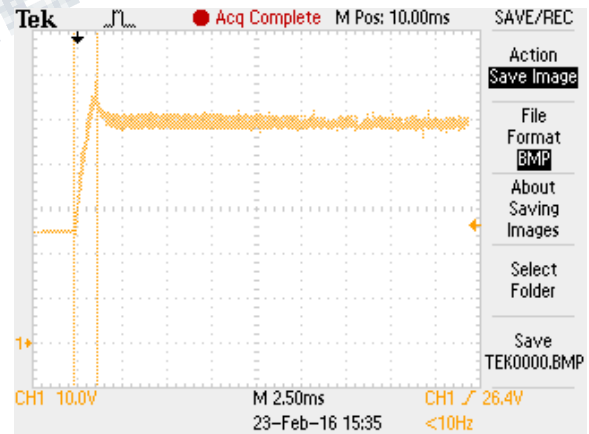
**Fig. 6 Damped filter**



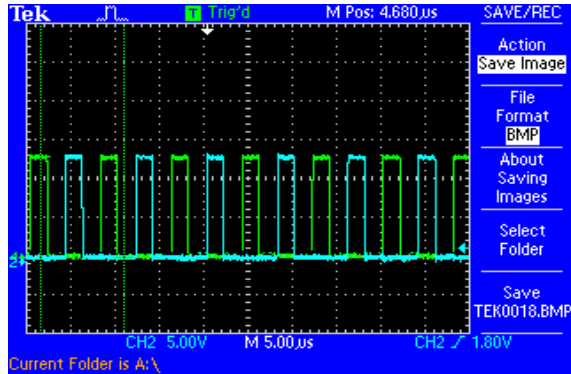
**Fig. 7 Filter interaction with the converter**

**V. EXPERIMENTAL RESULTS:**

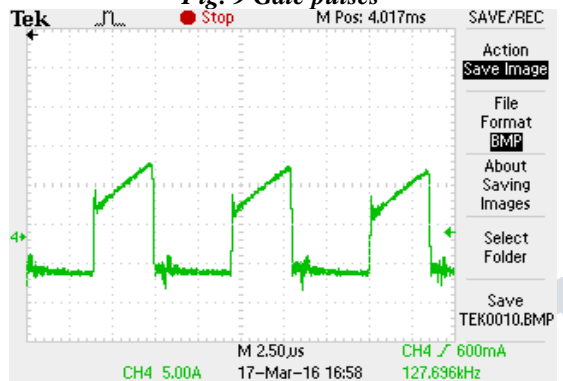
A prototype of boost converter with voltage mode PWM IC UC1825 has been built and tested. The complete test setup view of proposed converter is as shown.



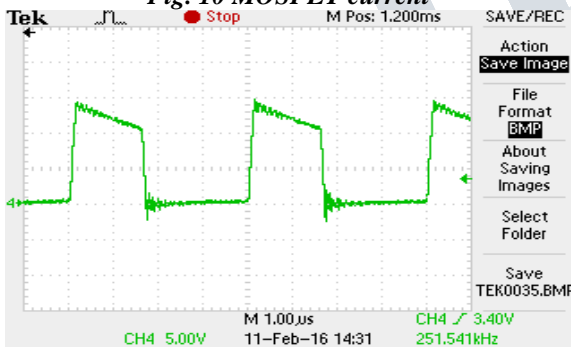
**Fig. 8 Output voltage**



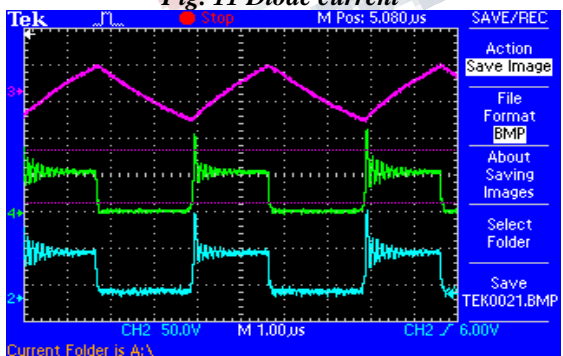
**Fig. 9 Gate pulses**



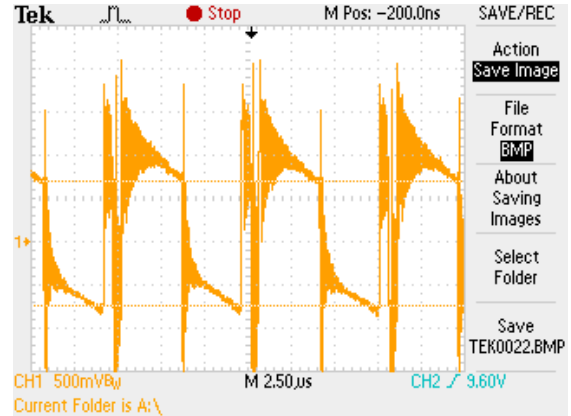
**Fig. 10 MOSFET current**



**Fig. 11 Diode current**



**Fig. 12 Inductor current and MOSFET voltages**



**Fig. 13 Output voltage ripple**



**Fig. 14 Experimental setup**

**VI. HARDWARE EXPERIMENTAL RESULTS:**

Table 1 and table 2 give experimental results of proposed converter.

**Line Regulation**

As the variation of output voltage with respect to varying input voltages for constant load current with full load.

Sl No	Vin(Volts)	Iin(Amps)	Vout(Volts)	Iout(Amps)
1	26	12.6	48.8	5.9
2	28	11.58	48.8	5.94
3	30	10.68	48.8	5.93
4	33	9.34	49	5.908

**Tables 1 experimental results of line regulation proposed converter**

**Load Regulation**

As the measure of variation of output voltage with respect to varying load current for a constant input voltage.

Sl No	Vin(Volts)	Iin(Amps)	Vout(Volts)	Iout(Amps)
1	26	2.01	50.8	1
2	26	6.31	50.4	3
3	26	12.6	48.8	6

**Tables 2 experimental results of load regulation**

### VI. CONCLUSION:

The boost converter is designed and implemented for the given specifications. The converter was designed for input range of 26 V to 33 V AC input voltage range, with 50V output, 300W full load output power and output voltage ripple less than 500mV. The converter designed is shown to work satisfactorily within given limits maintaining constant regulated output with minimal ripple. The load regulation is shown to be very low, hence demonstrating the converter's ability to account for variations in supply voltage and load to maintain constant (regulated) output. The circuit is simulated using ORCAD and the relevant waveforms are obtained.

### VII. ACKNOWLEDGMENT:

I express my sincere gratitude to Mr. Naveenkumar, Assistant professor, Department of Electrical and Electronics Engineering, Siddaganga Institute of Technology, Tumkur for his encouragement, valuable suggestions and motivation to work with this project. I am highly indebted to Mr. Venugopal B, Deputy Manager and Mr. Gummadi Srikanth ,Deputy Engineer ((CD & E, Power Supply Department), Bharat Electronics Limited, Bengaluru ,for their valuable guidance , constant supervising and also for giving necessary information concerning the project as well as for their constant support in finishing the project.

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