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# Novel Asymmetric Hybrid 15 Level Inverter with Reduced Number of Switches Using Different PWM Techniques – Part 1 Simulation Studies

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***Abstract:*** **- This paper proposes a best modulation technique is phase opposition and disposition pulse width modulation for the asymmetric multi-level inverter (AMLI) which is used for high voltage and high power with renewable energy sources. Here AMLI is used has higher voltage levels with reduced number of switches and dc sources. In this proposed 15-level hybrid AMLI have been implemented sinusoidal pulse width modulation (SPWM) and fundamental frequency pulse width modulation technique (FPWM) is used to achieve the stepped switched staircase waveform with quality of power output. The percentage of total harmonic distortion values of the hybrid AMLI are analyzed by using different PWM techniques are PDPW, APODPWM, PODPWM and PSPWM among these techniques phase opposition and disposition pulse width modulation is best technique is based on selective reduction in harmonic content and it can be produced higher number of output levels and number of phases. Simulation has been carried out using MATLAB/SIMULINK.**

***Keywords*-Asymmetric Multi-level inverter (AMLI), Total harmonic distortion (THD), PWM method**

## I. INTRODUCTION

The multilevel inverter was first introduced in 1975. The three level converters was the first multi- level inverter introduced [1]. A multilevel is a static power electronics circuit that synthesizes stepped form of output voltage from several levels o input dc voltages. With an increasing number of levels in output voltage of an inverter, output waveform approaches to sinusoidal waveform [2].

Multi-level inverters have more ability to perform well in high power source to medium voltage source with various industrial and renewable energy sources. The advantages of MLI are like reduced dv/dt stress, it can reduced less THD on output voltage stages comparison of two level cascaded inverter with MLI can operates higher voltage levels [3]. When the multi switching operation is occurred in the Output of MLI produces a sinusoidal stair case waveform, therefore less installation cost and filter design costs are induced. The output voltages of inverter are controlled by AC system. That is fed by multi- level inverter are used by traction system, motor drives and grid connections [4]. These applications are indices high power MLI operation at minimum high power switching frequency and fundamental switching frequency of MLI topology consists of 2 major types. One is symmetric multi-level inverter (SMLI) and another one is asymmetric multi-level inverter (AMLI). Compared to these two methods AMLI is more efficient advantages over the SMLI. Because it produces more output levels with less number of switches with different values of voltage sources. As the consideration of result it gives less no of H-bridges, gives less THD and circuits makes less space and cost is less compared to SMLI [5] [6] [7].

This paper deals with how higher levels output voltage is achieved for a new modified inverter topology using multicarrier based FPWM and SPWM techniques. This topology has the advantages of its reduced number of switching devices compared to the conventional cascaded H-bridge topology for the same levels. The modes of operations are outlined for fifteen -level inverter, as similar modes can be realized fifteen higher levels. Simulation of proposed fifteen-level inverter topology is carried out in MATLAB/SIMULINK software.

## II. ASYMMETRIC CASCADED MULTI CELL INVERTER

Cascaded multilevel inverter topology introduced single phase converter, it allows different dc sources it is based on the series connection. When compared to diode

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clamped and capacitor clamped cascaded MLI, it requires least number of semiconductor switches, dc voltage source and less H-bridges. From this new basic unequal dc voltage source cascaded topology, 15-level inverter consists of three H-bridges, three DC voltage sources. Fig:1 This conventional or existing asymmetric multilevel inverter have three different values of voltage sources and twelve power switches (MOSFET) to produce output of fifteen level waveform. In this case 'n' switches are necessarily to produce 2n+1 level in the output stage .The proposed cascaded hybrid asymmetric multilevel inverter it consists of seven semiconductor switches and voltage sources of V1 = Vdc, V2 = Vdc/2, V3 = Vdc/4 and (V1 =6V, V2=12V, V3=24V) which shown in Fig.2. The overall output voltage for fifteen level hybrid inverter is V (t )= V1 (t)+V2 (t)+V3 (t) which is based on opening switches and closing of switches S1,S2 and S3. The unequal dc voltage source converter is having three dc voltage sources, three power switches and three diodes along with a full bridge inverter configuration for switches S4, S5, S6, and S7. The Switches can be operated by both positive half cycle and negative half cycle of the output voltages and zero voltage. The proposed cascaded H- bridge inverter can gives positive, negative and zero or reference voltage levels. In upper leg or lower leg in the H-bridge system all switches are conducting in on state and the obtained output zero voltage. In output voltage levels are obtained by proper switching between the conducting switches. In this table 1, shows switching pattern for conventional AMLI operated in corresponding switches are get turned on to respective voltage and zero voltage indices OFF switching state.

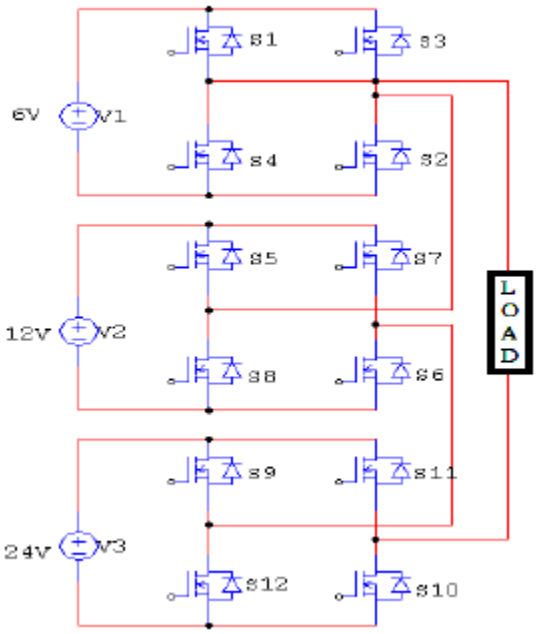


*Fig 1.Conventional Asymmetric multilevel inverter*

***Table 1. Switching pattern for conventional AMLI***

| S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 | S11 | S12 | OUTPUT VOLTAGE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | +Vdc |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | +2Vdc |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | +3Vdc |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | +4Vdc |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | +5Vdc |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | +6Vdc |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | +7Vdc |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0Vdc |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | -Vdc |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | -2Vdc |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | -3Vdc |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | -4Vdc |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | -5Vdc |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | -6Vdc |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | -7Vdc |

## III. PROPOSED TOPOLOGY

This proposed system induced new hybrid technique of cascaded multilevel inverter topologies, it requires less number of power devices sources depends on the output voltage level. In general, increased the number of semiconductor switches also increases the inverter circuit complexity, effective cost, installation space and control complexity as well as output voltage levels. Higher output voltage levels are needed to reduced the higher order THD in output voltage without adding filters. Thus to provide a large number of output levels without increasing the number of h-bridges, a new power circuit topology and a suitable method to determine the dc voltage sources level for asymmetrical 15 level output and asymmetrical multilevel inverter are proposed in this paper Fig. 2 shows the proposed basic unit for asymmetrical multilevel inverter. The output for 15-level topology is shown in below figure.

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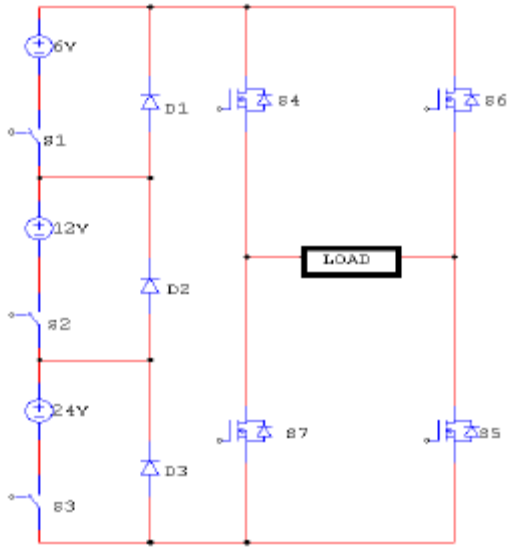


*Fig 2.Proposed Asymmetric multilevel inverter*

## IV. MODES OF OPERATION

The proposed topology includes seven modes in positive cycle and seven modes in negative cycle. The modes of operations as follows,

***MODE1:***

In this mode proposed circuit gives the output voltage of +Vdc. The load current comprises of S1, V1 ,S4, load ,S5, diodes D3 and D2. The output voltage is given by
*V0=V1=Vdc*

***MODE2:***
Here the switches S2, S4, S5 are turned ON and the output voltage obtained is +2Vdc. The current follows the path S2, V2, D1, S4, load, S5 and D3. The output voltage is given by
*V0=V2=2Vdc*

***MODE3:***
In this mode switches S1,S2,S4,S5 are turned ON and to get voltage level of +3Vdc. The current follows the path S2,V2,S1,V1,S4,load S5 and D3. The output voltage is given by
*V0=V1+V2=+3Vdc*

***MODE4*:**
In this mode proposed circuit gives the output voltage of +4Vdc. The load current comprises of S3,V3,D2,D1,S4,Load,S5. The output voltage is given by
*V0=V3=+4Vdc*

***MODE5:***
Here the switches S1,S3,S4,S5 are closed and the output voltage obtained is +5Vdc. The load current comprises of S3,V3,D2,S1,V1,S4,load and S5.The output is given by
*V0=V1+V3=+5Vdc*

***MODE6:***
In this mode proposed circuit gives the output voltage of +6Vdc. The current path is given by S3,V3,S2,V2,D1,S4,load and S5. The output voltage is given by
*V0=V2+V3=+6Vdc*

***MODE7:***
Here the switches S1,S2,S3,S4,S5 are closed. The output voltage obtained is +7Vdc and is given by
*V0=V1+V2+V3=+7Vdc*

**MODE8:**
In this zero voltage level is obtained. To get zero level no voltage source is connected to load. This is obtained by closing switches S5 and S6.

***Table 2.Switching Pattern For Proposed AMLI***

| S1 | S2 | S3 | S4 | S5 | S6 | S7 | OUTPUT VOLTAGE |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | +Vdc |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | +2Vdc |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | +3Vdc |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | +4Vdc |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | +5Vdc |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | +6Vdc |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | +7Vdc |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0Vdc |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | -Vdc |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | -2Vdc |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | -3Vdc |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | -4Vdc |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | -5Vdc |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | -6Vdc |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | -7Vdc |

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## V. MODULATION TECHNIQUES FOR ASYMMETRIC MULTILEVEL INVERTER

### *A . Hybrid Modulation Technique*

This is the newly developed modulation technique. The main characteristic of this hybrid modulation is used to generate a stepped switched waveform in the output voltage. This modulation contains high power quality and minimum harmonic content. The proposal in this project combines such a modulation strategy with fundamental frequency modulation (FPWM) and sinusoidal (SPWM).

### *B. FPWM Technique for H-Bridge Switches*

This technique is control the frequency of the output current or voltage. This frequency determines the speed of the motor. In this modulation output waveform approaches a nearly sinusoidal waveform and it reduces switching losses.

### *C.SPWM Technique For Asymmetric Basic Unit Switches*

Sinusoidal pulse width modulation technique is known as triangulation, used in industrial applications. In this technique a high frequency triangular carrier wave is compared with the sinusoidal reference wave consists of the switching action it is to be noted that by controlling the modulation index and control the amplitude of applied output voltage.

### *D. Multi Carrier Based PWM Techniques*

The carrier based pulse width modulation concept is based on the comparison of modulating signal (Reference) with a high frequency triangular waveform (carrier). This carrier signals can have unipolar or bipolar waveform. The switching instant is determined by the intersection of the carrier signal and modulating signal

### *E. Phase Opposition And Disposition PWM*

In this technique all the carriers signals are above and below zero reference line are in out of phase by 180º. This PODPWM technique is vastly used in conventional and multilevel converters because it provides has all carrier signals are same frequency and adjustable amplitudes with lower order harmonic distortion. When all the carriers are selected are in the same phase and opposite phase then this method is call it has a phase opposition and disposition pulse width modulation. In this method the voltage has quarter wave symmetry and odd wave symmetry due to the line voltage spectrum. In these three PWM techniques that are APOD, PD and POD produces similar forms of line and phase voltage waveforms. , for all of these PWM techniques, decision signals have Average frequency is lower than the carrier frequency. When the converter switch to +Vdc/2 the sine wave will be greater than both carrier waveforms, when converter is switch to +Vdc/4 the sine wave will be lower than upper most carrier waveform and greater than all other carriers, when converter switch to zero, sine wave will be lower than upper carrier but higher than lower carrier. When converter is switch to –Vdc/4 sine wave will be higher than lowermost carrier waveform and lesser than other carriers and when converters switch to sine wave will be less than both carrier waveforms.

Amplitude modulation index ma and frequency modulation index mf for this technique are

$$mf=fc/fr \quad \text{..... (1)}$$

$$ma=2Ar/(m*Ac) \quad \text{.....(2)}$$

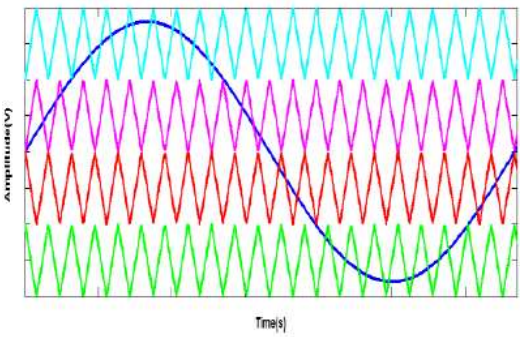


*Fig 3. Carrier and reference signal for PODPWM*

## VI. SIMULATION RESULTS

Simulation studies of the proposed AMLI with hybrid PWM strategies are performed by using MATLAB/SIMULINK. The simulation is carried out using MATLAB/SIMULINK. It is shown in the fig:.4. The simulation parameters are follows.

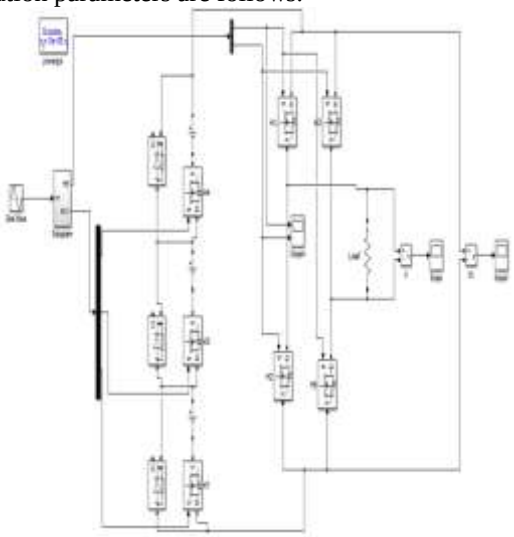

*Fig 4. Simulink model of AMLI*

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*Table 3. Simulation Parameters*

| SL.NO | Parameters | Voltage |
|---|---|---|
| 1 | Dc source V1 | 6V |
| 2 | Dc source V2 | 12V |
| 3 | Dc source V3 | 24v |
| 4 | Fundamental frequency, $f_f$ | 3150 Hz |
| 5 | Load resistance, R | 10 ohm |
| 6 | Switching frequency, fs | 50Hz |

The gating signal pattern for the seven switches is given by hybrid modulation technique employing POD technique. The gating signal pulse for three switches from asymmetric basic unit is given by SPWM and is shown in fig: 5.

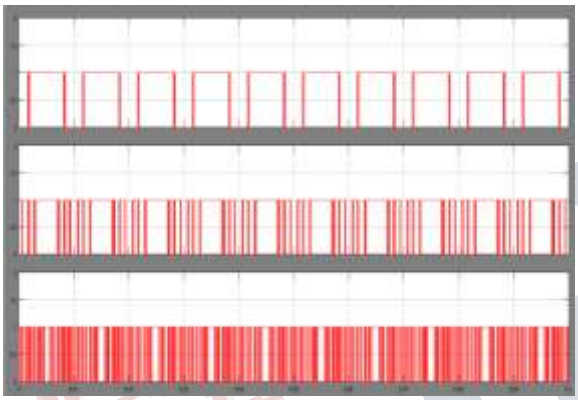

*Fig 5. Gating pulses by SPWM using POD for S1, S2, S3 switches*

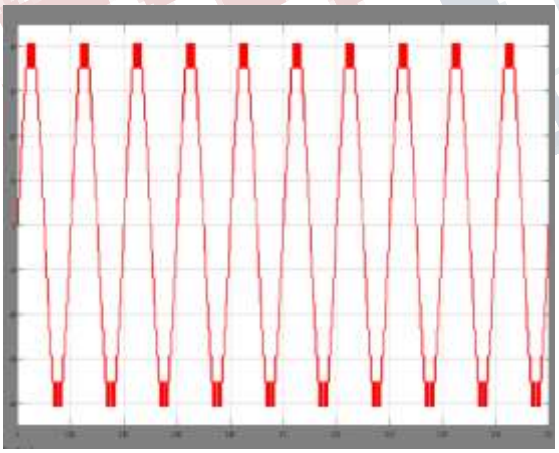

*Fig 6. Simulation output for PWM based AMLI with PODPWM*

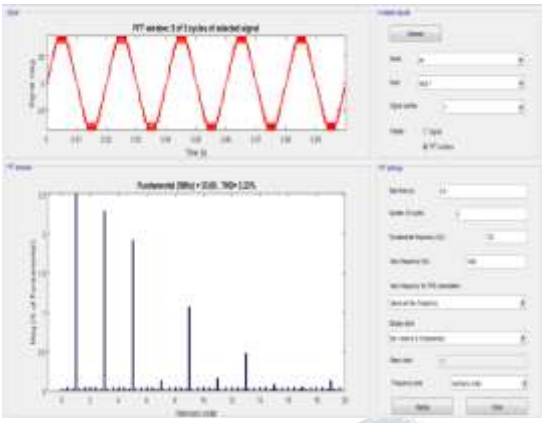

*Fig 7. FFT spectrum of modified fifteen- level inverter*

Fig:7 show the output voltage waveform for fifteen level AMLI with R-load employing POD modulation technique. The FFT simulation analysis is compared with various modulation techniques is initially calculated on the THD values and the result is PODPWM technique is the best method in reduced the minimum harmonic distortion. The FFT analysis for output voltage waveform of PODPWM is produced reduced THD waveform results are compared with different modulation techniques to find out the best one.

## VII. CONCLUSION

For the proposed system 15–level hybrid AMLI are used in industrial applications. In this new structure of a 15-level AMLI is consists of hybrid modulation strategies. In general, using these methods to reduce the lower order harmonics and reduced switching frequency modified hybrid PWM control methods has been implemented. It also provided a comparison of conventional cascaded multi-level inverter system with modified proposed hybrid AMLI. Over all these configuration we considered as POD(phase opposition and disposition) is proved the best control method to reduce the less THD and it can developed higher number of output levels and it requires number of phases. So that proposed AMLI topology performance and operation is obtained by the simulation and analysis of 15-level hybrid AMLI.

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