ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 2, Issue 8, August 2016

Power Quality Improvement for Multiple Output SMPS Based On Bridgeless Converter

[1] Jestin P J, [2] Mrs.Preethi Sebastian, [3] Mrs.Jeepa K J
[1] PG Scholar, [2] Associate Professor, [3] Assistant Professor
Mangalam College of Engineering, Ettumanoor, Kerala

Abstract: **In this paper design, analysis and simulation of new power factor correction multiple output switched mode power supply based on bridgeless buck-boost converter is proposed. Conventional SMPS with diode bridge rectifier has disadvantages such as high distortion in input current and low power factor. In order to rectify this problem new bridgeless converter based SMPS is proposed. Comparing with conventional topologies the proposed topology improves power quality indices. The performance evaluation of multiple output SMPS is done by varying input voltage. The performance of this SMPS is simulated in MATLAB/simulink environment.**

Index Terms— **Multiple output switched mode power supply (SMPS), Discontinuous conduction mode, DC-DC converter, power factor.**

I. INTRODUCTION

Switched mode power supply (SMPS) are extensively used in various application such as machine tools, industrials securities, support supplies with PLCs and personal computers. Switched mode power supplies (SMPS) commonly employed to power up the different parts in personal computer (PCs). It is economical to use multiple output SMPS for different output voltage levels rather than using single DC-DC converters for each voltage range. Multiple outputs of SMPS is mainly applicable for PCs to power up USB, Mouse, monitor and many digital and analog circuits. Normally in SMPS, diode bridge rectifier followed with capacitor filter at front end are used to convert AC to DC,DC-DC converter and high frequency transformer is used for obtaining isolation, multiple outputs and voltage scaling. This topology leads to poor power quality of the system mainly high THD (Total harmonic distortion), low power factor, poor voltage regulation, high conduction losses & high crest factor for AC input current.[1] Due to increasing awareness of power quality many manufactures related to power supply implemented power factor correction circuit at utility interface side so that they can maintain power quality standards as stated by IEEE 519 & IEC 61000 [2]-[3]. This became serious problem when large numbers of PCs are connected at common point, due effect like overloading of neutral conductor, noise, voltage distortion & de-rating of transformer [4].

In order to overcome these problems improved power quality SMPS are researched that they should be capable of drawing the sinusoidal current with high power factor. For obtaining improved power quality performance power factor correction (PFC) circuit is adopted in SMPS at the point of utility interface [5]-[7]. So single stage and two stage conversion of AC voltage to DC voltage is takes place in personal computer which will help for maintaining harmonic contain within limits. PFC is employed in power supplies able to provide low harmonic distortion, high power factor at different operating condition. Also they provide better output voltage regulation. For single- stage SMPS, normally AC input supply is given to the diode bridge rectifier (DBR) whose output is processed by multiple output PFC isolated dc-dc converter of dc output voltage [8]. Drawback of this type of SMPS is that it uses high value capacitor at the output and also produces stress on the components. Thus to overcome these problems two stage SMPS is preferred. Two stage SMPS is commonly used solution for medium power rating SMPS application personal computer (PCs).In this type first stage is used for enhancing power quality at the point of common coupling and the second stage is exclusively used for regulation output voltage. In order to get satisfactory performance power factor correcting circuit is used at front side, which will help for drawing input current sinusoidal with voltage so it will results in increases power factor as well as low harmonic distortion in current. The next important thing is to decide in which mode front end converter should operate. If cost is criteria for selection then discontinuous conduction mode (DCM) is selected for operation otherwise continuous conduction mode is selected. Because in CCM extra voltage and current sensor is required for sensing which makes it costlier. Also operation converter in DCM reduces the stress on devices. So for better operation PCs front end converter is designed in DCM.

In power factor correction circuit boost converter is commonly choice which is used in various industrial application, but major drawback of this is in cannot be used over wide input voltage range of ac supply [9]. In the same way buck converter also limited range of application for computer power supply due to its limitation in output voltage range [10].Recent growth in the power electronics has disable the us diode bridge rectifier at front side, which will results in improvement in power quality at input ac side. There are different types of bridgeless converter topologies are been researched such as CUK converter ,single ended primary inductance converter are to proposed which will reduces the conduction losses, better thermal management and low stress on components [11-13].As dealing with this converters, components count is increased for low power SMPS application. Wei et al. have presented bridgeless buck-boost
converter, in that topology it uses three switches which increase the conduction losses as well as component in the

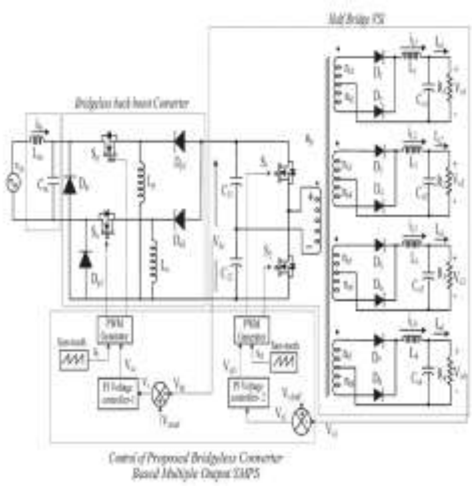

Fig 1.Circuit diagram of proposed system

Circuit Computer power supply require multiple outputs for its operation ,for getting multiple output half bridge voltage source inverter is used. For isolation of output high frequency transformer is used. Advantage of using this type of transformer is better utilization of core which cost effective solution as given in [14-17].

It can be stated that from available literature bridgeless converter topology has not been used for the switched mode power supply. So in this paper we made an attempt for improving the power quality of input ac supply which is degraded due to operation of SMPS in personal computers. Operations of bridgeless buck boost converter eliminate use of diode bridge rectifier, so that input current drawn by the converter is in phase with the supply voltage. In proposed two stage multiple output switched mode power supply bridgeless buck –boost converter is operate for both positive as well as negative cycle as a first stage in second stage regulated output voltage of dc-dc converter is given to the half bridge voltage source inverter in which high frequency transformer is used for isolation and for getting multiple outputs. The advantage of this configuration is that it reduces requirement of sensors to sense the input voltage and current due to operation of dc-dc converter in discontinuous conduction mode. Detailed design, analysis and performance is given following sections.

II. CIRCUIT CONFIGURATION OF MULTIPLE OUTPUT SYSTEM

In this configuration it involves two buck boost converter, PFC,voltage source inverter ,high frequency transformer, high frequency switches, diodes. Following diagram shows detailed arrangement of each components When single phase AC supply is given to the input of two buck –boost converter then high frequency component in supply is eliminated with help of L-C filter.Lin &Cin as shown in figure during operation this buck –boost converter which is placed at upper side is conducted with help of one high-frequency switch Sp, inductor Lp, and two diodes Dp1andDp2. Similarly, the bottom buck–boost converter that operates during the negative half cycle consists of one high frequency switch Sn, inductor Ln, and two diodes Dn1and Dn2 and lower converter is conducted for negative half cycle. [1].Both the inductor in converter designed in such way that they should ensure the Discontinuous mode operation of converter so that it will improve power factor of the sub sytem.now in the operation of voltage source inverter capacitor placed at input side of VSI acts as filter for DC output of buck-boost converter. closed control loop technique is employed for controlling the output of DC converter. This regulated output voltage is feed to the voltage source inverter for obtaining multiple output. The half-bridge VSI consists of two input capacitorsC11and C12, two high-frequency switchesS1andS2, and one multiple output high-frequency transformers (HFT). The HFT is consist of one primary winding and four secondary windings which are connected in center-tapped configuration to reduce the losses[1].inductor L1,L2,L3 L4 and capacitor C01,C02,C03,C04 are used to limit the ripples present in voltage and current. Highest output voltage is sensed for controlling purpose of voltage source inverter.

III. WORKING OF MULTIPLE OUTPUT SMPS

In our system consists of two back to back connected buck boost converter, voltage source inverter, multiple output high frequency transformer. The buck boost converter is designed for obtaining high power factor and low THD. The operation of converter for one switching cycle is given as follows,

A. Working of Buck-Boost Converter

The proposed bridgeless converter consists of two switches which is conducted for the positive and negative half cycles of the ac voltage respectively. This converter is operated in discontinuous mode DCM mode of operation to achieve high power factor. The DCM operation takes place in three stages. In the first stage when the first switch is ON the inductor associated with it starts storing energy and then inductor current increases to its maximum value. In the second state when the switch get turned off the inductor starts for discharging through capacitor hence inductor current decreases to minimum value. In the last state neither diode nor switches are conduct so that inductor current becomes zero and ensure DCM operation. The same sequence of operation takes place for negative half cycle.

B. Working of half bidge VSI

The output of buck-boost converter is controlled DC voltage which is given to half bridge VSI for voltage multiplying, isolation and for obtaining multiple outputs. The functioning of half bridge VSI for one switching cycle is shown in four stages. In the first stage when the upper switch is turned ON the input current flows through the primary of the transformer and to the lower capacitor. During this period diodes D1,D3,D5,D7 are forward biased so the current will flow through the respective inductor and it starts increasing. In the second mode both the switches are turned OFF and all diodes comes in freewheeling mode. Now the inductor current starts decreasing. In the third mode the lower switch is turned ON and current will flows through upper capacitor and primary of the transformer. The diodes D2,D4,D6,D8 will conduct and the inductors starts storing energy. When the inductor current becomes maximum the switch is turned OFF. The last state is similar to second state and same operation is continued.

IV. DESIGN OF MULTIPLE OUTPUT SMPS

In order to simulate the proposed converter model it is necessary to estimate the component values. All the switches and diodes are considered as ideal components. Very high switching frequency is selected here compared to line frequency.

A. Design of input filter

The higher order harmonics in the proposed SMPS is filtered by using LC filter. The input AC supply is directly given to this filter. Therefore a maximum value of capacitance is calculated.

$$C_{inmax} = \frac{I_m \tan\theta}{\omega V_m}$$

Where Vm and Im are peak ac voltage and current. We get 409nF as the capacitor value.

In order to obtain low harmonic distortion at the input side the filter inductor is calculated as

$$L_{in} = \frac{1}{4 * \pi^2 * Fc^2 * C_{in}}$$

Where Fc is a cut off frequency. The value for inductor is 3.07mH.

B. Design of Buck-Boost PFC converter

To ensure DCM operation the inductors in the Buck-Boost converter should be designed in such a way that it satisfies the conditions. The value of inductor is designed based on the change in the input current in one switching cycle. The ripple current is given by

$$L_p = \frac{DTV_{avg}}{\Delta i L_{pon}}$$

Where D is the duty cycle.

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 2, Issue 8, August 2016

The inductor current ripple is maximum in DCM which is equal to twice the input current.

$$\Delta iL_{pon} = 2 * I_{in}$$

When substituting the values we get as 607µH but to ensure DCM inductor value is considered as 60µH.

C. Design of half bridge Inverter

To eliminate the harmonics the input capacitors of the half bridge VSI acts as low pass filter so the design of input capacitor is done accordingly to eliminate the harmonics produced by AC supply. The input voltage and current should be in phase for maintaining PFC operation.

$$C = \frac{I_{dc}}{2\omega\Delta V_{dc}}$$

The input capacitors C11 and C12 are having same value which is calculated as 0.63mF.
For calculating turns ratio

$$n = \frac{V_{o1}}{D_d V_{dc}}$$

V. SIMULATION RESULTS

The simulation is done in MATLAB. The input voltage given is 220V and switching frequency, fs=40kHz. The designed values of input inductors Lp & Ln = 60_H. The designed values of filter capacitor Cin=330nF. Filter inductor takes the value Lin=2.5mH. Capacitors C11&C12=660_F. Control pulses are generated with the help of pulse generator.

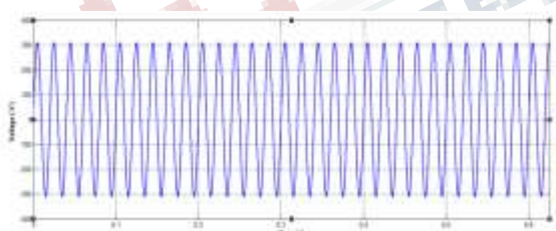

Fig 2. Input voltage waveform

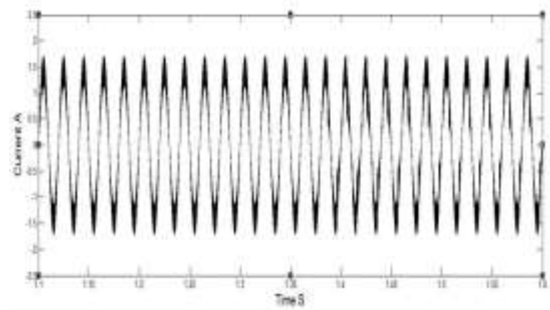

Fig 3. Input current waveform

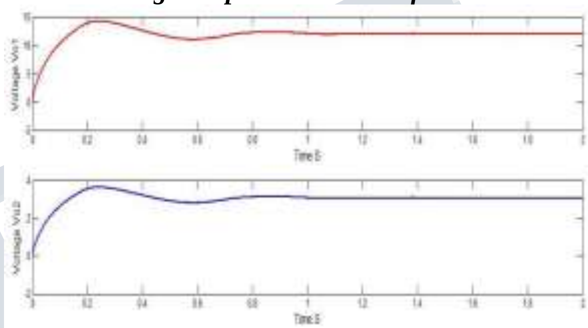

Fig 4. Output voltages waveform

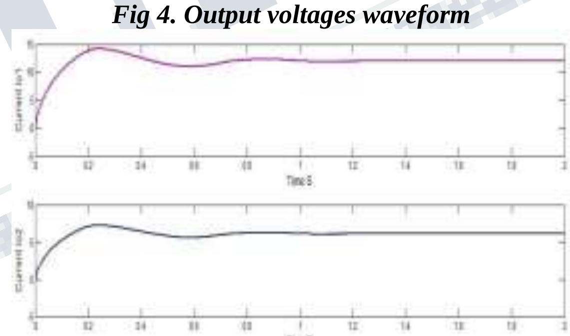

Fig 5. Output currents waveform

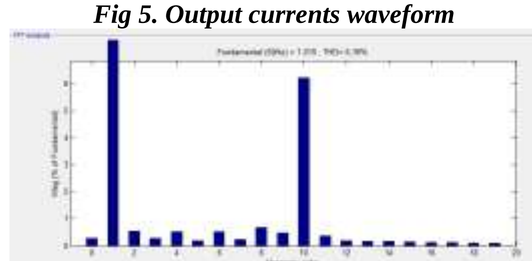

Fig 6. THD of the proposed system

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 2, Issue 8, August 2016

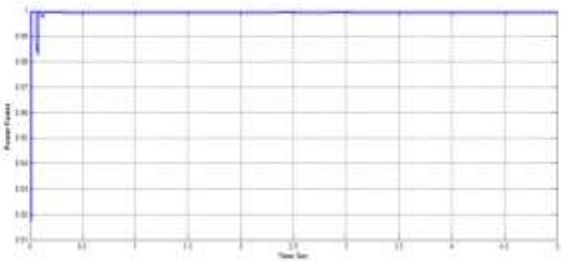

Fig 7. Power Factor of the proposed system

A. Performance under varying input voltages.

INPUT VOLTAGE	POWER FACTOR	THD
170 V	*0.9993*	*6.39%*
220 V	*0.9991*	*7.95%*
270 V	*0.9983*	*10.61%*

While varying the input voltage we get an improved power factor and THD from the system without large variations in the results..

B. Comparison with different systems.

CONVERTER	POWER FACTOR	THD
DBR	*.8898*	*123.72%*
Boost	*.9278*	*59.86%*
Buck Boost	*.9967*	*35.68%*
CUK	*.9531*	*68.41%*
Proposed System	*.9991*	*7.95%*

When power quality of the system is compared with the conventional systems it is clear that our system gives improved results.

VI. CONCLUSION

The bridgeless converter based multiple output SMPS gives good power quality performance. All the power quality measurements are well within the limits set by IEC-3-2. This SMPS gives the better voltage regulation due to use of buck boost converter. Operation of buck boost converter in discontinuous mode gives better power factor and reduction in the total harmonic distortion. The multiple output SMPS maintained constant voltage irrespective of changes in the supply voltages. While comparing the proposed converter with different conventional converters we came to know that proposed converter has better characteristics. The proposed system shows more better result than conventionally SMPS so it is recommended solution to computer power applications.

REFERENCES

1]. N. Mohan, T. M. Undeland, and W. P. Robbins, Power Electronics: Converters, Applications and Design. Hoboken, NJ,USA: Wiley,2003.

[2]. Limits for Harmonic Current Emissions, International ElectroTechnical Commission Standard, Std. 61000-3-2, 2004.

[3]. IEEE Recommended Practices and Requirements for Harmonics Controlling Electric Power System, IEEE Std. 519, 1992.

[4]. D. O. Koval and C. Carter, "Power quality characteristics of computerloads," IEEE Trans. Ind. Appl., vol. 33, no. 3, pp. 613–621,May/Jun. 1997.

[5]. Singh, S. Singh, A. Chandra, and K. Al-Haddad, "Comprehensive study of single-phase AC–DC power factor corrected converters with high frequency isolation,"IEEE Trans. Ind. Informant., vol. 7, no. 4, pp. 540–556, Nov. 2011
.
[6]. A. Canesin and I. Barbi, "A unity power factor multiple isolated outputs switching mode power supply using a single switch," in Proc.IEEE APEC, Mar. 1991, pp. 430–436.

[7]. K. Matsuiet al., "A comparison of various buck–boost converters and their application to PFC," inProc. 28th IEEE IECON, 2002, vol.1, pp. 30–36

[8]. Singh, S., Bhuvaneswari, G., Singh, B.:'Design, modeling,simulation and performance of a MOSMPS fed from a universal standard Single-phase outlet'. Int. Conf. on Power Electronics, Drivesand Energy Systems (PEDES) & Power India, 2010, pp. 1–6

[9]. H.-S. Kim et al., "On/Off control of boost PFC converters to improve light-load efficiency in paralleled power supply units for servers," IEEE Trans. Ind. Electron., vol. 61, no. 3, pp. 1235–1242, Mar. 2014

[10]. M. A. Dalla Costa, J. M. A. Álvarez, J. Garcia, A. L. Kirsten and D. G. Vaquero, "Microcontroller-based high-power-factor electronic ballast to supply metal halide lamps,"IEEE Trans. Ind. Electron., vol. 59,no. 4, pp. 1779–1788, Apr. 2012.

[11]. E. H. Ismail, "Bridgeless SEPIC rectifier with unity power factor and reduced conduction losses," IEEE Trans. Ind. Electron., vol. 56,no. 4

[12]. A. A. Fardoun, E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "Newefficient bridgeless Cuk rectifiers for PFC applications," IEEE Trans.Power Electron., vol. 27, no. 7, pp. 3292–3301, Jul. 2012

[13]. M. Mahdavi and H. Farzaneh-Fard, "Bridgeless Cuk power factor correction rectifier with reduced conduction losses,"IET Power Electron.,vol.5,

[14]. J. Y. Lee, G. W. Moon, and M. J. Youn, "Design of a power factor correction converter based on half bridge topology,"IEEE Trans. Ind. Electron., vol. 46, no. 4, pp. 710–723, Aug. 1999

[15]. J. M. Kwon, W. Y. Choi, H. L. Do, and B. H. Kwon, "Single stage half bridge converter using a coupled inductor,"IEE Proc.- Elect. Power Appl., vol. 152, no. 3, pp. 748–756, Apr. 2005

[16]. W.-Y. Choi and J.-S. Yoo, "A bridgeless single stage half bridge AC/DCconverter,"IEEE Trans. Power Electron., vol. 26, no. 12, pp.3884–3895,Dec. 2011.