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Suppression of Common Mode Voltage and Differential Mode Harmonics in Three Phase Inverter Using Hybrid Filter

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Abstract: **-- In this paper, a hybrid filter is presented to reduce the CM voltage (CMV) and the differ-ential-mode (DM) harmonics in a three-phase inverter with carrier peak position modulation (CPPM). Because the use of CPPM strategy in the inverter can ensure that the output CMV will be only two levels in any condition, the simple active CM filter (composed of a half-bridge circuit) in the hybrid filter can effectively suppress the output CMV and CM current. The passive filter in the hybrid filter consists of an added single tuned filter and the original DM low-pass filter. The single tuned filter is designed to lower the DM harmonics, which are aggravated by the CPPM strategy in the carrier frequency band. Through the experiments, the validity of CMV and DM harmonics suppression by the hybrid filter in the three-phase inverter is verified and the calculation-control active CM filter is proved to be the best in the optional schemes.**

Index Terms**—Carrier peak position modulation (CPPM), common-mode voltage (CMV), differential-mode (DM) harmonics, hybrid filter, sinusoidal pulse width modulation (SPWM).**

I. INTRODUCTION

In the motor regulation systems driven by pulse width modulation (PWM) inverters, the peaks of output common-mode (CM) voltage are very high due to the instantaneous imbalance of three phase voltages. The CM voltage (CMV) will produce a huge pulsating CM current (CMC) through the distributed capacitance of the system. The CMC could interfere with the adjacent devices along the ground wire and even will result in the wrong operation of the devices[1], [2]. For the inverter with the discontinuous PWM (DPWM) strategy, the CMV is reduced by avoiding the generation of zero vectors. Under different carrier polarity combinations there are different DPWM methods [11], [12], such as active zero state PWM (AZSPWM) [13], remote state PWM (RSPWM) [14], [15], near state PWM (NSPWM).

For the sinusoidal PWM (SPWM) control inverter, the CMV can be reduced by using the carrier phase shift (CPS) strategy [17]. In order to break through the limitation of the modulation index, the strategy of carrier peak position modulation (CPPM) is adopted [18].When the zero state appears, instead of the usual symmetric triangular carrier, an oblique triangular carrier is used to modulate the reference voltage. Thus, the zero state is avoided and the CMV is reduced.

When the system is established, the CMV *dv/dt* plays a decisive role in the CMC. In the inverter system, the peak value of the output CMC is influenced by the CMV *dv/dt* and the distributed capacitance of the system. In aforementioned strategies, although all the output CMVs of inverters can be reduced to ±*V*dc/6 (*V*dc is the dc-side voltage of inverters), the step level of CMV is still *V*dc/3 when their switches are switching. CM filters can be divided into passive and active ones.

Active CM filters are of more popular concern. In some active filters, the active devices are working in the linear region and the reversal voltage is produced to compensate the CMV of the three-phase inverter. Most passive filters are realized with two common ways: a CM choke or CM transformer cascading into the main circuit; a resistor-capacitor (RC) or resistor-inductor-capacitor (RLC) attenuation network paralleling into the main circuit. The drawbacks of passive CM filters are as follows: its bulky size, high power loss, etc. The active filter is implemented by using a multi-level inverter and the four-level voltage is yielded to counteract the CMV. In the conventional SPWM or SVM three-phase inverter, the CMV is a four-level pulse. . In the

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above active filters, all the compensative voltages are cascaded into the inverter's output through a CM transformer. Under the CPPM strategy, the output CMV of the inverter will be only two levels in all cases. So the active CM filter in the hybrid filter is designed to be a simple half-bridge structure, which can be used to counteract almost all the CMV. The single tuned filter and the existing low-pass filter form a passive DM filter. Thus the hybrid filter is designed not only to suppress the CMV but also to make the DM voltage (DMV) comply with standards. In Section II, the CMV in the three-phase inverter is reviewed briefly. Section III presents the fact that the phase-shifting of the carrier affects the output DMV of the inverter in theory and shows the simulation results accordingly. In Part A of Section IV, the designing process of the active CM filter is expounded. The single tuned filter is shown in Part B of Section IV. The implementation of the hybrid filter is discussed in Part C of Section IV. The experimental results of the three-phase inverter with or without the hybrid under different strategies are compared in Section V.

II. CMV IN THREE-PHASE INVERTER

In the three-phase inverter as shown in Fig. 1, the output CMV *vcm* can be expressed as

$$Vcm = (va+vb+vc)/ 3 \quad (1)$$

where *va*, *vb*, and *vc* are the output voltages of three legs respectively.

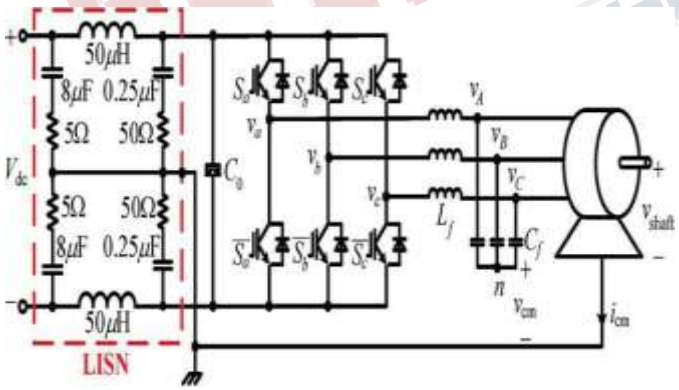

Fig. 1. Three-phase inverter

Fig. 2(a) shows the CMV in the three-phase inverter with the conventional SPWM strategy. When *va*, *vb*, and *vc* are of high (or low) level, which is called the zero state, the peaks of the output CMV are maximal (about ±*V*dc/2). The zero state is the major cause of the huge CMV. If the peaks of three carriers are mutually staggered *Tc*/3 (*Tc* is the carrier cycle) in the inverter, the probability for the occurrence of the zero state will be the lowest. As shown in Fig. 2(b), the occurrence frequency and the duration time of ±*V*dc/2 in CMV are reduced greatly. In order to avoid the zero state in all cases, the variant oblique triangular carrier is used to modulate the reference sinusoidal voltage instead of the usual symmetric triangular carrier in the inverter with the CPPM strategy. Fig. 2(c) shows that the peaks of the output CMV with CPPM are reduced to ±*V*dc/6. The problem of the switching dead-time has been considered in the calculation of carrier peak positions.

III. HARMONICS OF DMV

For the asymmetrical regular-sampled SPWM, the output voltage of Phase *r* (*r* = *a*, *b*, *c*) in the three-phase inverter can be expressed by (2) [32]. In (2), *Jn*[•] is the *n*th order Bessel function; *f*0 is the output power-frequency; *m* is the carrier index; *n* is the baseband index; *q* = *m* + *nf*0/*fc*; *θrc* and *θr*0 are the initial phases of the carrier and the reference sinusoid respectively. the DMV *vab* between Leg A and Leg B of the three-phase inverter under the conventional SPWM strategy can be deduced. Its result is revealed in (3). In the similar manner, the DMV under the CPS strategy can be got by (4).

$$V_r(t)=\frac{2}{\pi}V_{dc}\sum_{\substack{m=0\\m>0}}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{q}j_n\left(\frac{qMa\pi}{2}\right)\sin\left[\left(\frac{(m+n)\pi}{2}\right)\right]\cos[m(2\pi f_c t+\theta_{rc})+n(2\pi f_0 t+\theta_{r0}] \quad (2)$$

$$v_{ab,SPWM}(t)=-\frac{4V_{dc}}{\pi}\sum_{\substack{m=0\\m>0}}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{q}j_n\left(\frac{qM_a\pi}{2}\right)\sin\left[(m+n)\frac{\pi}{2}\right]\sin\left(n\frac{\pi}{3}\right)\sin[2\pi(mf_c+nf_0)t-n\pi/3] \quad (3)$$

$$V_{ab,CPS}(t)=-\frac{4V_{dc}}{\pi}\sum_{\substack{m=0\\m>0}}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{q}j_n\left(\frac{qM_a\pi}{\pi 2}\right)\sin\left[(m+n)\frac{\pi}{2}\right]\sin\left((m+n)\frac{\pi}{3}\right)\sin\left[2\pi(mf_c+nf_0)t-(m+n)\pi/3\right] \quad (4)$$

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TABLE I
INITIAL PHASES OF DIFFERENT LEGS

Strategy	Leg A		Leg B		Leg C	
	θ_{ac}	θ_{a0}	θ_{bc}	θ_{b0}	θ_{cc}	θ_{c0}
Conventional SPWM	0	0	0	-2π/3	0	2π/3
CPS	0	0	-2π/3	-2π/3	2π/3	2π/3

Under different strategies, the DMVs of the three-phase inverter with no-load (i.e. load impedance is infinite) are simulated. The simulated parameters are listed in Table II. The output DMV behind *Lf Cf* filter in the three-phase inverter.

TABLE II
SIMULATED PARAMETERS IN THREE-PHASE INVERTER

Symbol	Value	Commentary
V_{dc}	700 V	DC-side voltage
L_f	900 μH	Inductor of low-pass filter
C_f	25 μF	Capacitor of low-pass filter
f_0	50 Hz	Output power-frequency

According to (4), the magnitude of DMV under the CPS strategy at *fc* will not be zero and even will be large. Although the harmonics of the output DMV will be somewhat reduced through the low-pass filter (see *Lf Cf* in Fig. 1), the total harmonic distortion (THD) of DMV would be serious and even be substandard when the designed carrier frequency is low.

The CPPM strategy is based on the CPS strategy. The difference between them is that the carrier peak position is changed for a short time in a small range [18]. Hence the output DMV harmonics in the inverter with CPPM will be similar to that with CPS. Table III lists the simulated DMV THDs under different carrier frequencies. Under the condition of low *fc*, if the CMV is suppressed by using the CPPM strategy, an extra DM filter is needed to reduce the harmonics in the carrier frequency band.

IV. HYBRID FILTER

A special design of DM filter aims at the suppression of the DMV harmonics in the carrier frequency band, because the DMV harmonics will make the THD exceed the standards. Using the CPPM strategy can ensure that the output CMV will be only two-level voltage in any case (see Section II). Thus, to suppress the CMV, a simple switching circuit can be designed as an active CM filter to produce the two-level voltage, which is the reversal of the original CMV.

A. Active CM Filter

In the design procedure of the active CM filter, the switch-ing circuit structure must be determined in accordance with the characteristic of the CPPM strategy firstly. Secondly, the coupling mode of the filter output must be designed. Lastly, the acquisition mode of the CMV signal must be selected. Because the output CMV in the inverter with CPPM is a two-level voltage, a single-phase inverter structure can be designed to

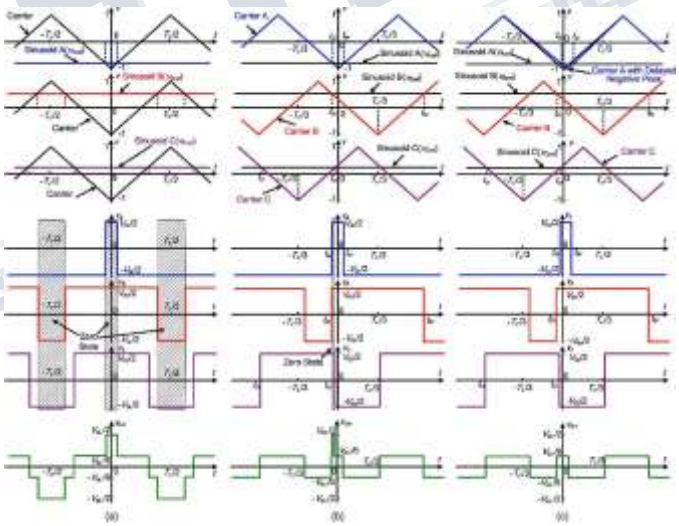

Fig. 2. Modulation of three-phase reference voltages with different carriers (top), three-phase output pulses (middle) and output CMVs (bottom) in the three-phase inverter under (a) the conventional SPWM strategy, (b) the CPS strategy, and (c) the CPPM strategy generate a reverse two-level voltage to the CMV.

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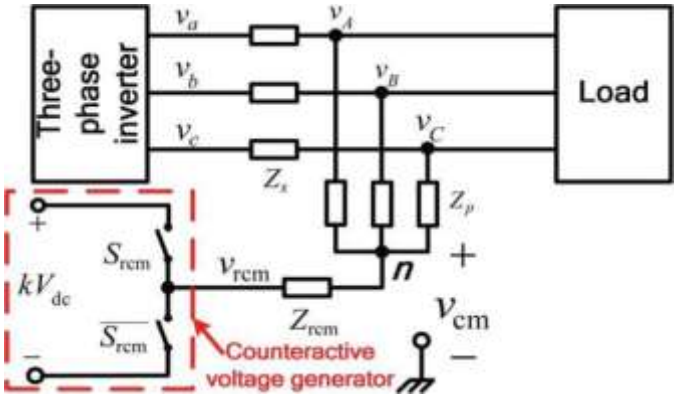

Fig. 3. Structure of the active CM filter

As shown in Fig. 3, the output voltage *v*rcm of the half-bridge is ±*k*Vdc/2. The counteractive voltage of the CMV can be generated. The class of the dc-side voltage in the active CM filter can be changed by the proportional coefficient *k*. This is useful for the flexibility in choosing switching devices. The active CM filter is coupled into the main circuit of the three-phase inverter is the output current of the active circuit is injected into the main circuit through the filter network in parallel (as shown in Fig. 3). The essence of this method is to change the potential of the neutral point *n* and to make it close to zero in theory.

According to Fig. 3, the CMV of the inverter's output is

$$v_{cm} = \frac{(v_a + v_b + v_c)Z_{rcm} + v_{rcm}(Z_s + Z_p)}{(Z_s + Z_p) + 3Z_{rcm}} \quad (6)$$

where *Z*rcm is the output equivalent impedance of the active cir-cuits in the filter network, and *Zs* and *Zp* are, respectively, the series impedance and the parallel impedance of the inverter's output. According to (6), if *v*rcm is controlled as follows

$$v_{rcm} = -Z_{rcm}(v_a + v_b + v_c)\,(Z_s + Z_p). \quad (7)$$

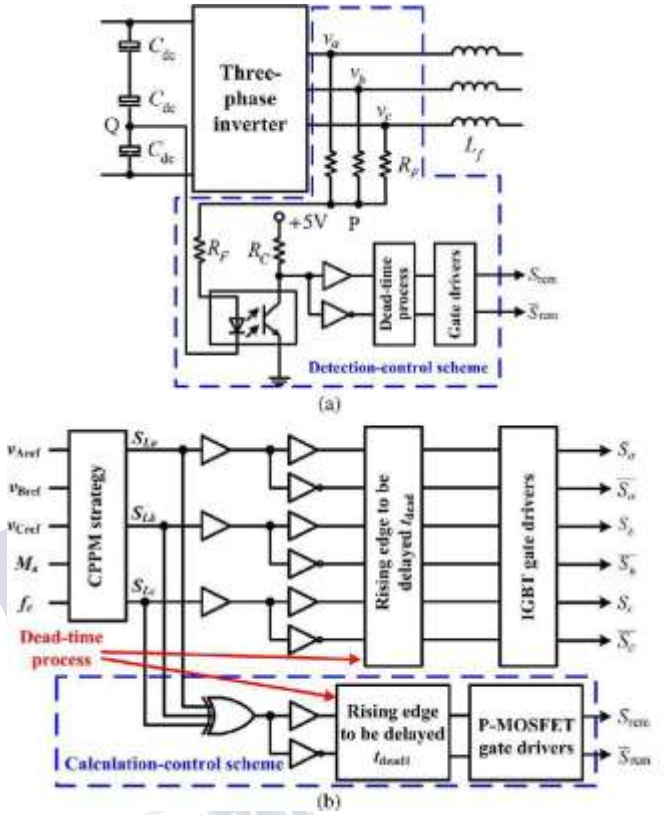

Fig. 5. Generation for the control signals of the active CM filter un- der (a) the detection-control scheme, and (b) the calculation-control scheme

*v*cm will be zero in theory. Because *v*rcm = ±*k*Vdc/2, *va* + *vb* + *vc* = ±*V*dc/2, and they are opposite to each other, the design results can be obtained as follows

$$v_{rcm} = -k(v_a + v_b + v_c) \quad (8)$$

$$Z_{rcm} = k(Z_s + Z_p). \quad (9)$$

According to (8), the control signal *S*rcm of an active filter's switch should have the reverse polarity to the signal *va* + *vb* + *vc*. Two schemes can be used to obtain the control signal *S*rcm. The first is the "detection-control" scheme. As shown in Fig. 5(a), the signal is from a Y-type CMV detection circuit, which is made up of three *Rp* resistors. It is connected to the logic circuit, the dead-time process circuit, and the gate driver through an optocoupler. One terminal of the optocoupler is Point P (its potential is ±*V*dc/6 under the CPPM strategy), the other is Point Q (its potential is −*V*dc/6). This

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scheme has two weak points. One is the delay from "detection" to "control." The other is that the active counteractive circuit has its own switching dead-time problem. To solve the former problem, a faster op to coupler can be adopted to detect the voltage and the signal process should be simplified as far as possible in the implementation.

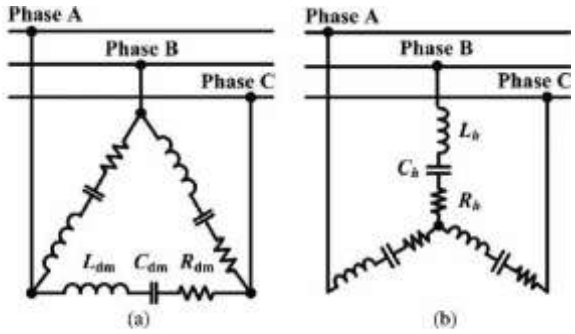

Fig. 5. Three-phase single tuned filter. (a) Δ -type and (b) Y-type.

The second way to obtain *S*rcm is the "calculation-control" scheme. Under this scheme, the signal *S*rcm is calculated in the processor as the following:

$$Srcm=SLa \oplus SLb \oplus SLc \ldots\ldots\ldots (10)$$

where *SLa*, *SLb* and *SLc* are the control logic signals of the top switches of Leg A, Leg B, and Leg C, respectively [see Fig. 4(b)]. The delay of the detection-control process is avoided and no extra detection circuit is needed by using this scheme. The output voltage *v*rcm with *S*rcm [by (10)] can not be guaranteed to be the reverse of *va* + *vb* + *vc* every moment either.

B. Passive DM Filter

As analyzed in Section III, the THD of the output DMV in the three-phase inverter with CPPM is substandard markedly when the carrier frequency is low. Since most harmonic energy locates in the carrier frequency band, filtering out the harmonics near the carrier frequency can greatly improve the DM characteristic of the inverter's output. What needs to be suppressed is mainly the carrier frequency harmonics, so a simple single tuned filter can be adopted to parallel in the line–line output of the three-phase inverter. There are two types of three-phase single tuned filters. In view of the connection with the active CM filter, the Y-type filter is better than the -type one. If the inductor *Lh* and the capacitor *Ch* in Fig. 5(b) are designed to satisfy the single tuned filter can greatly suppress the harmonics near the carrier frequency.

$$F_c = 1 \Big/ \left(2\pi\sqrt{L_h C_h}\right)$$

C. Hybrid Filter

The hybrid filter in the design plan (see Fig. 6). In Fig. 6, the proportional coefficient *k*, which is mentioned in Part A of Section IV, is set 1/3. From Fig. 7, it can be seen that the mid-point of the inverter dc input is equipotential with the ground in essence because of the Line Impedance Stabilization Network (LISN). Then the voltage at any point is equal to the potential difference from the point to the mid-point of the dc input. Because the output CMVs of the inverter with the CPPM strategy are ±*V*dc/6, the dc input voltage levels of the active CM filter must also be ±*V*dc/6 when *k* = 1/3. So the dc voltage of the active filter can be taken from the divided voltage of the inverter dc voltage through the middle capacitor which is one of the series capacitors on the inverter dc-side. The potentials of the middle capacitor's two ends are just ±*V*dc/6. It will form an organic whole to connect the above designed active CM filter with the passive DM filter through the neutral point n.

TABLE IV
EXPERIMENTAL PARAMETERS IN THREE-PHASE INVERTER

Symbol	Value	Commentary
V_{dc}	700 V	DC-side voltage
L_f	900 μH	Inductor of low-pass filter
C_f	25 μF	Capacitor of low-pass filter
L_h	90 μH	Inductor of single tuned filter
C_h	22 μF	Capacitor of single tuned filter
R_h	0.09 Ω	Resistor of single tuned filter
R_p	1 MΩ	Resistor for detecting CMV
R_f	230 kΩ	Current-limiting resistor
R_L	4.7 kΩ	Pull-up resistor
L_{f1}	300 μH	Inductor of active filter
L_{f2}	30 μH	
C_{f1}	75 μF	Capacitor of active filter
C_{f2}	66 μF	
R_f	0.03 Ω	Resistor of active filter
f_0	50 Hz	Output power-frequency
f_c	3.6 kHz	Carrier frequency
t_{dead}	5 μs	Switching dead-time of IGBT
t_{dead1}	1 μs	Switching dead-time of P-MOSFET

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$Lr1 = Lf/3$, $Cr1 = 3Cf$, $Lr2 = Lh/3$, $Cr2 = 3Ch$, and $Rr = Rh/3$. The detailed parameters are listed in Table IV.

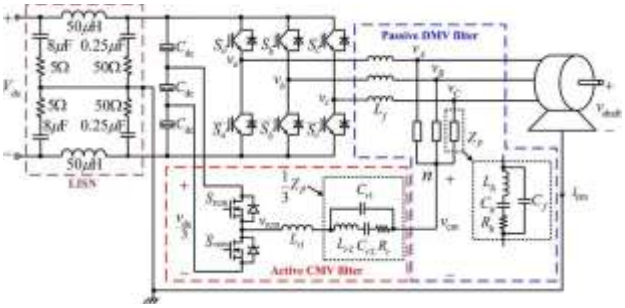
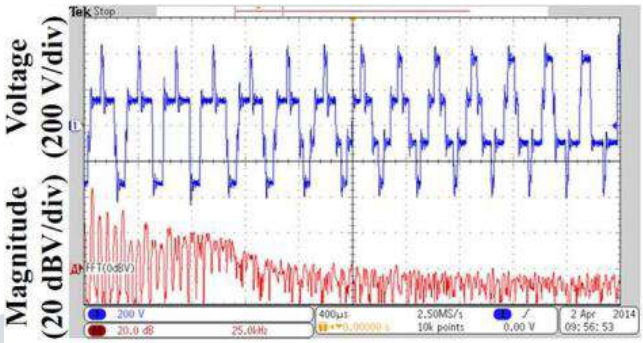


Fig.6. Three-phase inverter with the hybrid filter.

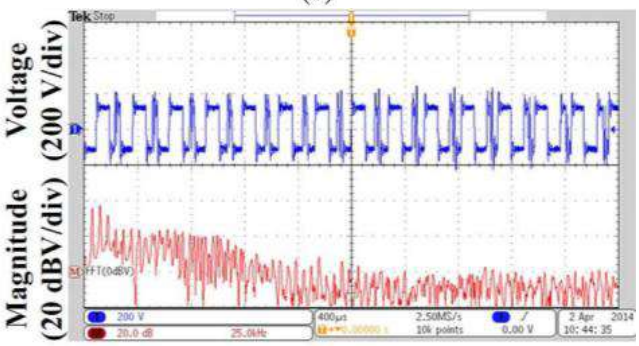
V. EXPERIMENTS

In the experiments, the switches of the inverter's main circuit are implemented by insulated-gate bipolar transistors (IGBTs) and the switches of the active CM filter are implemented by P-MOSFETs. An induction motor, whose rated voltage is 380 V and rated power is 3 kW, is used as the load of the inverter. The other parameters of the experimental circuit (see Fig. 6) are listed in Table IV. In the experiments, the detection-control scheme and the calculation-control scheme are implemented respectively in the processor as the control signals of the active filter's switches.

In the three-phase inverter with CPPM, the detection-control scheme and calculation-control scheme are adopted to drive the hybrid filter respectively. To ensure that the experiments are carried out under the same load conditions, the detection-control module [as shown in Fig. 4(a)] is still retained in the main circuit when the active CM filter is driven by the calculation-control scheme block [as shown in Fig. 4(b)].The output CMV *v*cm, CMC *i*cm, and DMV *v*AB are measured under the above two schemes. In order to observe the influence of the CMV on the motor shaft, the shaft voltages *v*shaft of the motor are measured by a carbon brush.
Fig. 7 shows the output CMVs of the inverter under different conditions. Fig. 7(a) shows that the peaks of CMV (above 350 V and below −350 V) will appear in every carrier cycle under the conventional SPWM strategy. Under the CPPM strategy, the CMV wave is generally between −117 V and +117 V. Even if the overshoot of the jump edges is taken into consideration, the CMV peaks are not outside the range of ±240 V [see Fig. 7(b)]. Under the CPPM strategy, the output CMVs of the inverter with the hybrid filter are shown in Fig. 7(c) and (d). By using the detection-control or the calculation-control hybrid filter, in the CMV there are only some spikes, whose duration is of microsecond level. The spikes do not exceed ±100 V. The FFT results in Fig. 7(c) and (d) show that the peak of the output CMV spectrum in the inverter with the hybrid filter is greatly lower than that without the hybrid filter [Fig. 7(b)].



(a)



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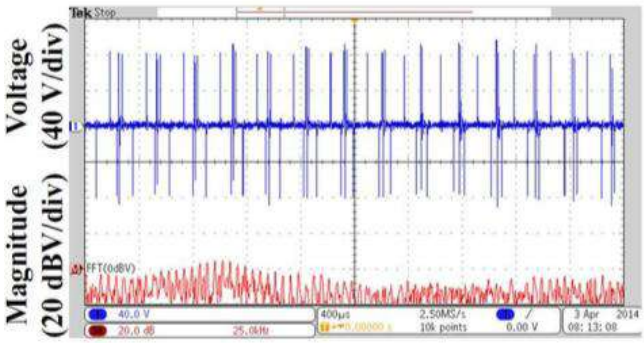

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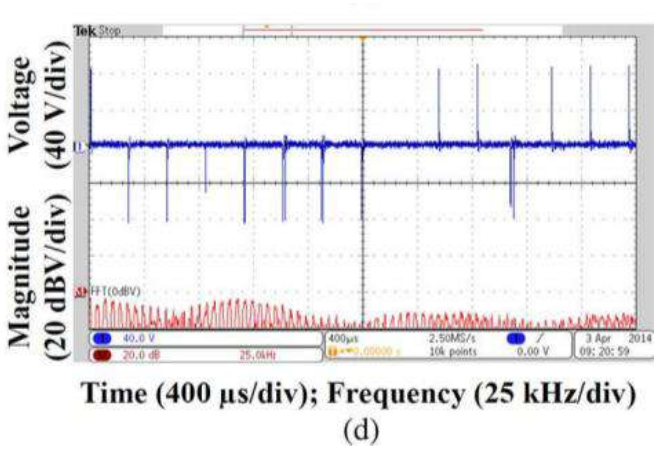

Fig. 7. Experimental results of the CMV *v*cm (top) and its FFT (bottom) in the three-phase inverter without a hybrid filter (a) under the conventional SPWM strategy or (b) under the CPPM strategy, and (c) with the detection-control hybrid filter or (d) with the calculation-control hybrid filter under the CPPM strategy.

The CMV results, the harm of the shaft voltage in the three-phase in-verter driven motor system with the hybrid filter is less than that without the hybrid filter. To drive the hybrid filter, the suppres-sion effect of the shaft voltage through the calculation-control scheme is better than that through the detection-control scheme.

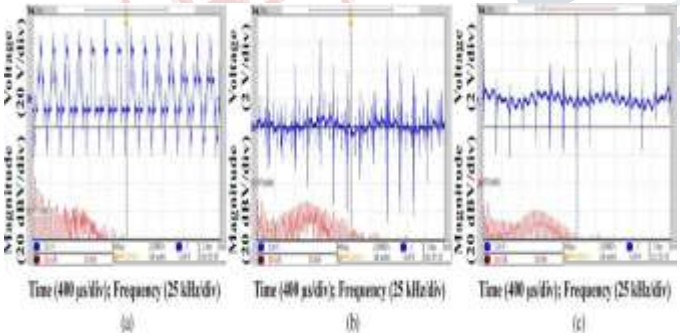

Fig. 8. Experimental results of the shaft voltage vshaft (top) and its FFT (bottom) in the three-phase inverter (a) under the conventional SPWM strategy without a hybrid filter, and under the CPPM strategy (b) with the detection-control hybrid filter or (c) with the calculation-control hybrid filter.

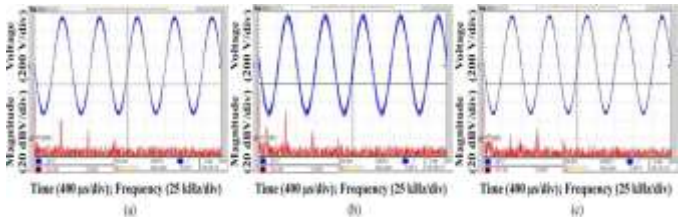

Fig. 9. Experimental results of the DMV vAB (top) and its FFT (bottom) in the three-phase inverter (a) under the conventional SPWM strategy or(b) under the CPPM strategy without a hybrid filter, and (c) under the CPPM strategy with the hybrid filter.

Fig.9 shows the output DMV *vAB* in the inverter under dif-ferent conditions. The FFT results in Fig.9(a) and (b) confirm the previous simulation conclusion: the major harmonics of the DMV are near the carrier frequency. Under the conventional SPWM strategy and the CPPM strategy without a hybrid filter, the maximal magnitudes of the DM harmonics are 20 dBV and 30 dBV respectively. As shown in Fig.9(c), the harmonic peak of the DMV in the carrier frequency band is reduced by more than 20 dBV while the hybrid filter is added. After using the hybrid filter, the THD under the CPPM strategy is reduced from above 9% to below 2.5%, which can meet the demand of most loads for the output AC voltage of the inverter.

VI. CONCLUSION

Through the above analysis and experiments, the hybrid filter, which is designed in this paper to suppress the CMV and DM harmonics of the three-phase inverter, is proved to have the following characteristics.

1. Simple in structure: Because it is ensured that the output CMV of the inverter can be two levels in any case by using the CPPM strategy, the simple half bridge is used in the hybrid filter to counteract the CMV. The simple structure means lower cost.

2. Flexible in application: The proportional coefficient k provides the flexibility for the application design of the hybrid filter in various power levels

3. Optimized in effect: As for the CMV suppression effect, the inverter with the hybrid filter is much better than that without the hybrid filter and the hybrid filter under the

calculation-control scheme is superior to that under the detection-control scheme.

4. Compatible in THD standard: A single tuned filter in the hybrid filter suppresses the harmonics well and makes the output sinusoidal volt-age meet the THD demand of loads.

REFERENCES

[1] Y. Murai, T. Kubota, and Y. Kawase, "Leakage current reduction for a high-frequency carrier inverter feeding an induction motor," *IEEE Trans. Ind. Appl.*, vol. 28, no. 4, pp. 858–863, Jul./Aug. 1992.

[2] G. L. Skibinski, R. J. Kerkman, and D. Schlegel, "EMI emissions of modern PWM AC drives," *IEEE Ind. Appl. Mag.*, vol. 5, no. 6, pp. 47–80, Nov./Dec. 1999.

[3] S. Chen, T. A. Lipo, and D. Fitzgerald, "Source of induction motor bear-ing currents caused by PWM inverters," *IEEE Trans. Energy Concers.*, vol. 11, no. 1, pp. 25–32, Mar. 1996.

[4] A. Muetze and A. Binder, "Calculation of circulating bearing currents in machines of inverter-based drive systems," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 932–938, Apr. 2007.

[5] F. J. T. E. Ferreira, M. V. Cistelecan, and A. T. de Almeida, "Evaluation of slot-embedded partial electrostatic shield for high-frequency bearing current mitigation in inverter-fed induction motors," *IEEE Trans. Energy Convers.*, vol. 27, no. 2, pp. 382–390, Jun. 2012.

[6] D. F. Busse, J. M. Erdman, R. J. Kerkman, D. W. Schlegel, and G. L. Skibinski, "The effects of PWM voltage source inverters on the mechanical performance of rolling bearings," *IEEE Trans. Ind. Appl.*, vol. 33, no. 2, pp. 567–576, Mar./Apr. 1997.

[7] R. S. Araujo, R. A. Rodrigues, H. de Paula, and L. M. R. Baccarini, "Premature wear and recurring bearing failures in three-phase induction motors: A case study," *IEEE Latin Amer. Trans.*, vol. 9, no. 4, pp. 528– 533, Jul. 2011.

[8] J. Espina *et al.*, "Reduction of output common mode voltage using a novel SVM implementation in matrix converters for improved motor lifetime," *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 5903–5911, Nov. 2014.

[9] T. D. Nguyen and H. H. Lee, "Modulation strategies to reduce common-mode voltage for indirect matrix converters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 129–140, Jan. 2012.

[10] N. Zhu, D. Xu, B. Wu, N. R. Zargari, M. Kazerani, and F. Liu, "Common-mode voltage reduction methods for current-source converters in medium-voltage drives," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 995– 1006, Feb. 2013.

[11] A. M. Hava and N. O. Cetin, "A generalized scalar PWM approach with easy implementation features for three-phase, three-wire voltage-source inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1385–1395, May 2011.

[12] A. R. Beig, S. Kanukollu, K. Al Hosani, and A. Dekka, "Space-vector-based synchronized three-level discontinuous PWM for medium-voltage high-power VSI," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3891– 3901, Aug. 2014.

[13] A. M. Hava and E. Un, "Performance analysis of reduced common-mode voltage PWM methods and comparison with standard PWM methods for three-phase voltage source inverters," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 241–252, Jan. 2009.

[14] M. Cacciato, A. Consoli, G. Scarcella, and A. Testa, "Reduction of common-mode currents in PWM inverter motor drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 2, pp. 469–475, Mar./Apr. 1999.

[15] M. Cavalcanti *et al.*, "Modulation techniques to eliminate leakage currents in transformerless three-phase photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 57, no. 4, pp. 1360–1368, Apr. 2010.