

Star Configuration Based Control Method for Transformer less H-Bridge Cascaded Statcom

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Abstract: This paper presents a transformer less static synchronous compensator (STATCOM) system based on multilevel H-bridge converter with star configuration. This proposed control method devote themselves not only to the current loop control but also to the dc capacitor voltage control. With regards to the current loop control, a nonlinear controller based on the passivity-based control (PBC) theory is used in this cascaded structure STATCOM for the first time. As to the dc capacitor voltage control, overall voltage control is realized by adopting a proportional resonant controller. Clustered balancing control is obtained by using an active disturbances rejection controller. Individual balancing control is achieved by shifting the modulation wave vertically which can be easily implemented in a field-programmable gate array. Two actual H-bridge cascaded STATCOMs rated at 10 kV 2 MVA are constructed and a series of verification tests are executed. The experimental results prove that H-bridge cascaded STATCOM with the proposed control methods has excellent dynamic performance and strong robustness. The dc capacitor voltage can be maintained at the given value effectively. **Index Terms**—Active disturbances rejection controller (ADRC), H-bridge cascaded, passivity-based control (PBC), proportional resonant (PR) controller, shifting modulation wave, static synchronous compensator (STATCOM)

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I. INTRODUCTION

(PCC) to absorb or inject the required reactive power, through which the voltage quality of PCC is improved [3]. In recent years, many topologies have been applied to the STATCOM. Among these different types of topology, H-bridge cascaded STATCOM has been widely accepted in high-power applications for the following advantages: quick response speed, small volume, high efficiency, minimal interaction with the supply grid and its individual phase control ability [4]–[7]. Compared with a diode-clamped converter or flying capacitor converter, H-bridge cascaded STATCOM can obtain a high number of levels more easily and can be connected to the grid directly without the bulky transformer. This enables us to reduce cost and improve performance of H-bridge cascaded STATCOM [8].

There are two technical challenges which exist in H-bridge cascaded STATCOM to date. First, the control method for the current loop is an important factor influencing the compensation performance. However, many no ideal factors, such as the limited bandwidth of the output current loop, the time delay induced by the signal detecting circuit, and the reference command current generation process, will deteriorate the compensation effect. Second, H-bridge cascaded STATCOM is a complicated system with many H-bridge cells in each phase, so the dc capacitor voltage imbalance issue which caused by different active power losses among the cells, different switching patterns for

different cells, parameter variations of active and passive components inside cells will influence the reliability of the system and even lead to the collapse of the system. Hence, lots of researches have focused on seeking the solutions to these problems.

II. CONFIGURATION OF THE 10 KV 2 MVA STATCOM SYSTEM

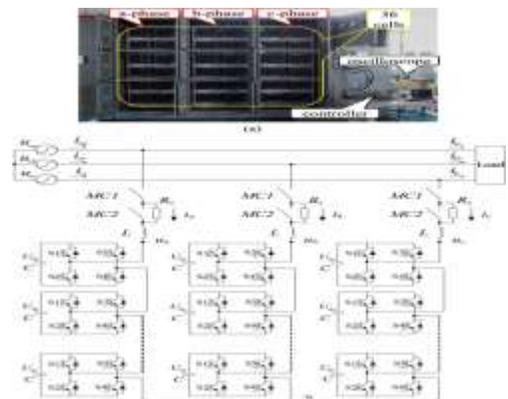


Fig. 1. Actual 10 kV 2MVA H-bridge cascaded STATCOM. (a) Experimental hardware view. (b) Configuration of the experimental system.

Fig. 1 shows the circuit configuration of the 10 kV 2 MV Astar-configured STATCOM cascading 12 H-bridge

pulse width modulation (PWM) converters in each phase and it can be expanded easily according to the requirement. By controlling the current of STATCOM directly, it can absorb or provide the required reactive current to achieve the purpose of dynamic reactive current compensation. Finally, the power quality of the grid is improved and the grid offers the active current only. The power switching devices working in ideal condition is assumed. $u_a, u_b,$ and u_c are the three-phase voltage of grid. $u_{sa}, u_{sb},$ and u_{sc} are the three-phase voltage of STATCOM. $i_{sa}, i_{sb},$ and i_{sc} are the three-phase current of grid. $i_a, i_b,$ and i_c are the three-phase current of STATCOM. $i_{la}, i_{lb},$ and i_{lc} are the three-phase current of load. U_{dc} is the reference voltage of dc capacitor. C is the dc capacitor. L is the inductor. R_s is the starting resistor.

Table I
Circuit parameters of the experimental system

Grid voltage	u_g	10 kV
Rated reactive	Q	2 MVA
AC inductor	L	10 mH
Starting resistor	R_s	4 kΩ
DC capacitor capacitance	C	5600 μF
DC capacitor reference voltage	U_{dc}	800 V
Number of H-bridges	N	12
PWM carrier frequency	f	1 kHz

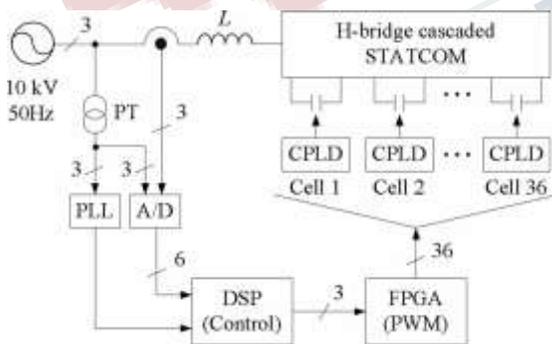


Fig. 2. Digital control system for 10 kV 2 MVA H-bridge cascaded STATCOM.

The modulation technology adopts the carrier phase-shifted sinusoidal PWM (abbreviated as CPS-SPWM) with

the carrier frequency of 1 kHz. Then, with a cascade number of $N = 12$, the ac voltage cascaded results in a 25-level waveform in line to neutral and a 49-level waveform in line to line. In each cluster, 12 carrier signals with the same frequency as 1 kHz are phase shifted by $2\pi/12$ from each other. When a carrier frequency is as low as 1 kHz, using the method of phase-shifted unipolar sinusoidal PWM, it can make an equivalent carrier frequency as high as 24 kHz. The lower carrier frequency can also reduce the switching losses to each cell.

III. CONTROL ALGORITHM

Fig. 3 shows a block diagram of the control algorithm for H-bridge cascaded STATCOM. The whole control algorithm mainly consists of four parts, namely, PBC, overall voltage control, clustered balancing control, and individual balancing control. The first three parts are achieved in DSP, while the last part is achieved in the FPGA.

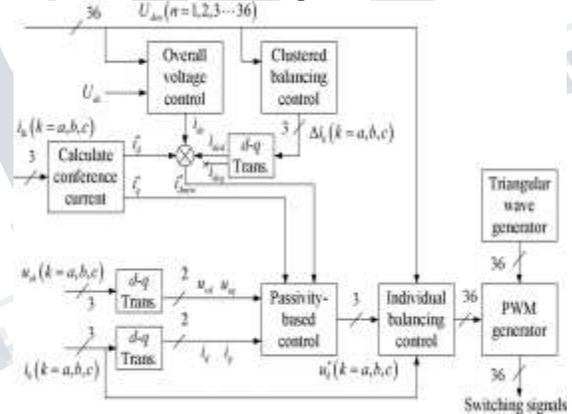


Fig. 3. Control block diagram for the 10 kV 2 MVA H-bridge cascaded STATCOM.

A. PBC

Referring to Fig. 1, the following set of voltage and current equations can be derived:

$$\begin{cases} L \frac{di_a}{dt} = u_{sa} - u_a - Ri_a \\ L \frac{di_b}{dt} = u_{sb} - u_b - Ri_b \\ L \frac{di_c}{dt} = u_{sc} - u_c - Ri_c \end{cases} \quad (1)$$

where R is the equivalent series resistance of the inductor. Applying the $d-q$ transformations (1), the equations in $d-q$ axis are obtained

$$\begin{cases} L \frac{di_d}{dt} = -Ri_d + \omega L i_q + u_{sd} - u_d \\ L \frac{di_q}{dt} = -\omega L i_d - Ri_q + u_{sq} - u_q \end{cases} \quad (2)$$

Equation (2) is written as the following form:

$$\begin{bmatrix} L & 0 \\ 0 & L \end{bmatrix} \begin{bmatrix} \frac{di_d}{dt} \\ \frac{di_q}{dt} \end{bmatrix} + \begin{bmatrix} 0 & -\omega L \\ \omega L & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} u_{sd} - u_d \\ u_{sq} - u_q \end{bmatrix} \quad (3)$$

Along with selecting i_d and i_q as state variables, it gives the following EL system model of (3):

$$M\dot{x} + Jx + Rx = u \quad (4)$$

where $x = [i_d \ i_q]$ is the state variable. $M = \begin{bmatrix} L & 0 \\ 0 & L \end{bmatrix}$ is the positive definite inertial matrix and $M = MT$. $J = \begin{bmatrix} 0 & -\omega L \\ \omega L & 0 \end{bmatrix}$ is the dissymmetry interconnection matrix and $J = -JT$. $R = \begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix}$ is the positive definite symmetric matrix which reflects the dissipation characteristic of the system. $u = \begin{bmatrix} u_{sd} - u_d \\ u_{sq} - u_q \end{bmatrix}$ is the external input matrix which reflects the energy exchange between the system and environment.

$$V \leq u^T y - Q(x) \dots \dots \dots (5)$$

Assume the energy storage function as (6) for H-bridge cascaded STATCOM

$$V = \frac{1}{2} x^T M x = \frac{1}{2} L (i_d^2 + i_q^2) \quad (6)$$

By taking the derivative of V and utilizing antisymmetric characteristic of J , (7) is obtained as follows:

$$\dot{V} = x^T M \dot{x} = x^T (u - Jx - Rx) = x^T u - x^T R x \quad (7)$$

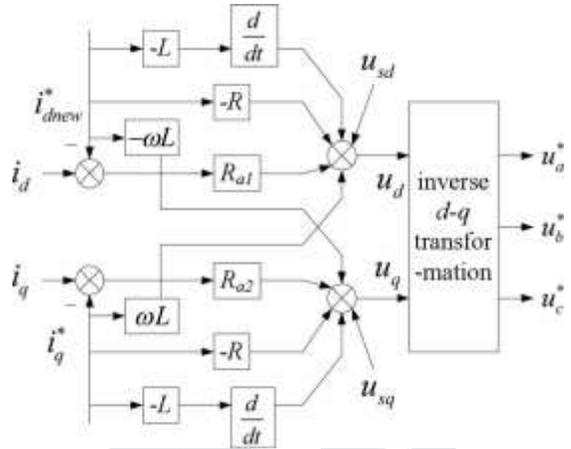


Fig. 4. Block diagram of PBC.

B. Overall Voltage Control

As the first-level control of the dc capacitor voltage balancing, the aim of the overall voltage control is to keep the dc mean voltage of all converter cells equaling to the dc capacitor reference voltage. The common approach is to adopt the conventional PI controller which is simple to implement. However, the output voltage and current of H-bridge cascaded STATCOM are the power frequency sinusoidal variables and the output power is the double power frequency sinusoidal variable, it will make the dc capacitor also has the double power frequency ripple voltage. So, the reference current which is obtained in the process of the overall voltage control is not a standard dc variable and it also has the double power frequency alternating component and it will reduce the quality of STATCOM output current.

$$G_{PR}(s) = k_p + \frac{2k_r \omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \quad --(8)$$

where k_p is the proportional gain coefficient. k_r is the integral gain coefficient. ω_c is the cutoff frequency. ω_0 is the resonant frequency. k_r influences the gain of the controller but the bandwidth. With k_r increasing, the amplitude at the resonant frequency is also increased and it plays a role in the elimination of the steady-state error. ω_c influences the gain of the controller and the bandwidth. With ω_c increasing, the gain and the bandwidth of the controller are both increased.

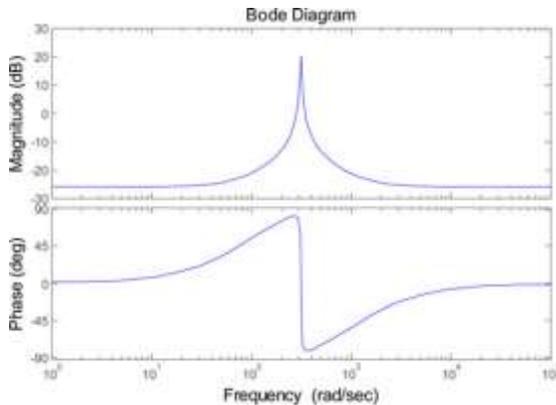


Fig. 5. Bode plots of the PR controller.

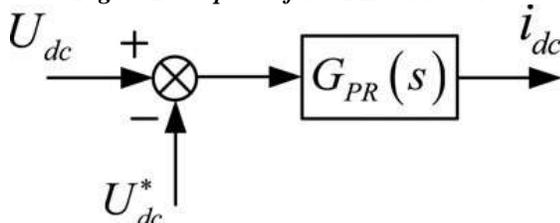


Fig. 6. Block diagram of overall voltage control.

C. Clustered Balancing Control

Taking the clustered balancing control as the second level control of the dc capacitor voltage balancing, the purpose is to keep the dc mean voltage of 12 cascaded converter cells in each cluster equaling the dc mean voltage of the three clusters. ADRC is adopted to achieve it. Then, it requires several steps to complete the design of ADRC for H-bridge cascaded STATCOM, which are as follows.

- 1) According to (1), H-bridge cascaded STATCOM is a first-order system; thus, the first-order ADRC is designed. Taking the dc capacitor voltage of each cluster as the controlled object for analysis, the clustered balancing control model is built and the input and output variables and the controlled variable of the controlled object are determined.
- 2) By using the nonlinear tracking differentiator (TD) which is a component of ADRC, the transient process for the reference input of the controlled object is arranged and its differential signal is extracted.

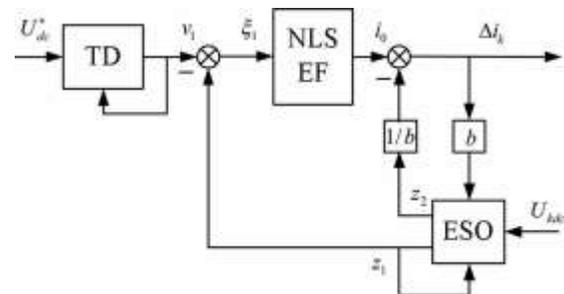


Fig. 7. Block diagram of clustered balancing control.

D. Individual Balancing Control

As the overall dc voltage and the clustered dc voltage are controlled and maintained, the individual control becomes necessary because of the different losses. The aim of the individual balancing control as the third level control is to keep each of 12 dc voltages in the same cluster equaling the dc mean voltage of the corresponding cluster. It plays an important role in balancing 12 dc mean capacitor voltages in each cluster. Due to the symmetry of structure and parameters among the three phases, a-phase cluster is taken as an example for the individual balancing control analysis. Fig. 8 shows the charging and discharging states of one cell. According to the polarity of output voltage and current of the cell, the state of the dc capacitor can be judged. Then, the dc capacitor voltage will be adjusted based on the actual voltage value.

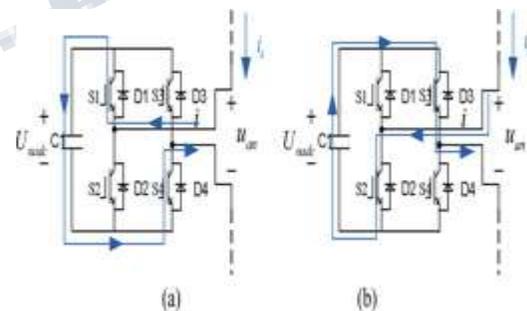


Fig. 8. Charging and discharging states of one cell.
 (a) Charging state. (b) Discharging state

The previous principle is also suitable for reducing discharging time and prolonging the charging and discharging times of the cell. Summing up the previous analysis, the method can be illustrated as follows. 1) If the requirement is to reduce the duty cycle, it needs to shift down the normal modulation wave and shift up the opposite modulation wave. 2) If the requirement is to prolong the duty

cycle, it needs to shift up the normal modulation wave and shift down the opposite modulation wave.

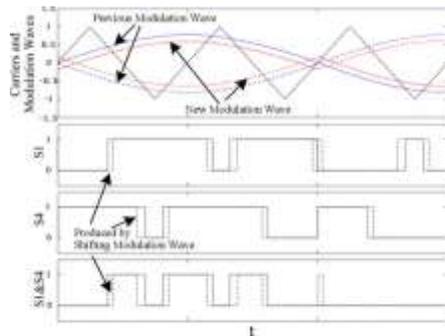


Fig. 9. Process of shifting modulation wave

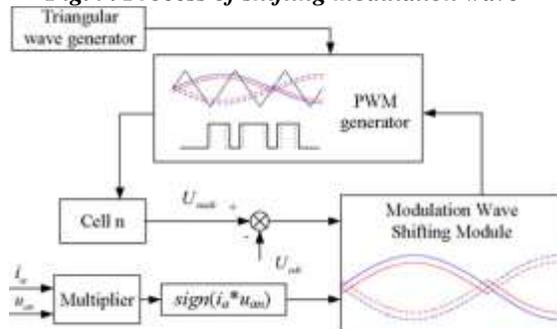


Fig. 10. Block diagram of individual balancing control.

IV. EXPERIMENTAL RESULTS

To verify the correctness and effectiveness of the proposed methods, the experimental platform is built according to the second part of this paper. Two H-bridge cascaded STATCOMs are running simultaneously. One generates the set reactive current and the other generates the compensating current that prevents the reactive current from flowing into the grid. The experiment is divided into two parts: the current loop control experiment and the dc capacitor voltage balancing control experiment. In current loop control experiment, the measured experimental waveform is the current of a-phase cluster and it is recorded by the oscilloscope. In dc capacitor voltage balancing control experiment, the value of dc capacitor voltages are transferred into DSP by a signal acquisition system and they can be recorded and observed by CCS software in computer. Finally, with the exported experimental data from CCS, experimental waveform is plotted by using MATLAB.

Current Loop Control Experiment

The current loop control experiment is divided into four processes: steady-state process, dynamic process, startup process, and stopping process. Fig. 12 shows the experimental results verifying the effect of PBC in steady-state process. As shown in Fig. 12(a), it is the experimental result of the full load test. With the proposed control method, the reactive current is compensated effectively. The error of the compensation is very small. The residual current of the grid is also quite small. The phase of the compensating current is basically the same as the phase of the reactive current. The waveforms of the compensating current and the reactive current are smooth and they have the small distortion and the great sinusoidal shape. As shown in Fig. 12(b), it is the experimental result of the over load test. When STATCOM is running in over load state (about 1.4 times current rating), due to the selected IGBT has been reserved the enough safety margin, STATCOM still can run continuously and steadily. The over load capability of STATCOM is improved greatly and the operating reliability of STATCOM in practical industrial field is enhanced effectively. However, considering the over load capability of other devices.

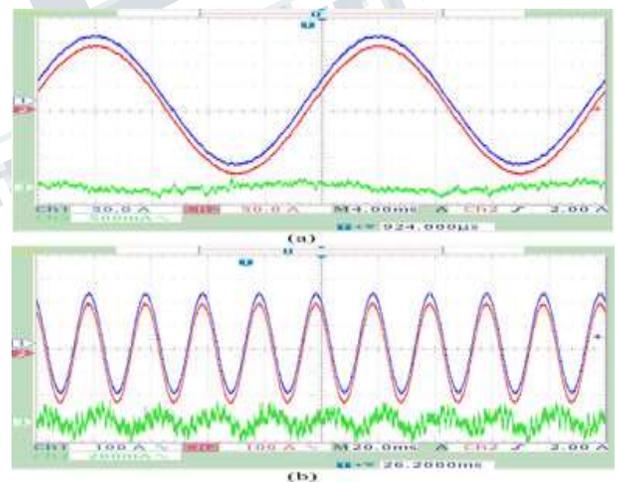


Figure 12 : Experimental results verify the effect of PBC in steady-state process. (a) Ch1: reactive current; Ch2: compensating current; Ch3: residual current of grid. (b) Ch1: reactive current; Ch2: compensating current; Ch3: residual current of grid.

Results of dc capacitor voltage balancing control show that the proposed control methods can coordinate with each other and achieve the best control effect. They also improve the steady state and dynamic performance of STATCOM

V. CONCLUSION

This paper has analyzed the fundamentals of STATCOM based on multilevel H-bridge converter with star configuration. And then, the actual H-bridge cascaded STATCOM rated at 10 kV 2 MVA is constructed and the novel control methods are also proposed in detail. The proposed methods have the following characteristics.

- 1) A PBC theory-based nonlinear controller is first used in STATCOM with this cascaded structure for the current loop control, and the viability is verified by the experimental results.
- 2) The PR controller is designed for overall voltage control and the experimental result proves that it has better performance in terms of response time and damping profile compared with the PI controller.
- 3) The ADRC is first used in H-bridge cascaded STATCOM for clustered balancing control and the experimental results verify that it can realize excellent dynamic compensation for the outside disturbance.
- 4) The individual balancing control method which is realized by shifting the modulation wave vertically can be easily implemented in the FPGA.

The experimental results have confirmed that the proposed methods are feasible and effective. In addition, the findings of this study can be extended to the control of any multilevel voltage source converter, especially those with H-bridge cascaded structure.

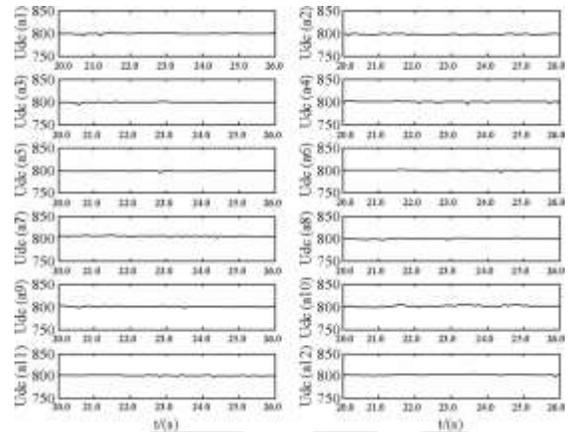


Fig. 17. Experimental waveforms of 12 cells in a-phase cluster for testing individual balancing control in the steady-state process

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