ISSN (Online) 2395-2717
International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 2, Issue 8, August 2016

A Quad Two-Level Inverter Topology

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Abstract: **-- A multilevel inverter topology for a four-pole induction-motor drive is presented in this paper, which is constructed using the induction-motor stator winding arrangement. A single dc source with a less magnitude when compared with conventional fivelevel inverter topologies is used in this topology. Therefore, power balancing is-sues (which are major challenges in conventional multilevel inverters) are minimized. As this configuration uses a single dc source, it provides a path for zero-sequence currents because of the zero-sequence voltages present in the output, which will flow through the motor phase winding and power electronic switches. To minimize these zero-sequence currents, sine–triangle pulse width modulation (SPWM) is used, which will shift the lower order harmonics near to switching frequency in the linear modulation region. However, in the case of over modulation, harmonic voltages will be introduced close to the fundamental frequency. In this regard, a modified SPWM technique is proposed in this paper to operate the drive in the over modulation region up to the modulation index of 2/√3. The proposed quad two-level inverter topology is experimentally verified with a laboratory prototype on a four-pole 5- hp induction motor. Experimental results show the effectiveness of the pro-posed topology in the complete linear modulation region and the over modulation region.**

Index Terms **— Induction motor drive, modified sine– triangle pulse width modulation (SPWM), multilevel inverter, over modulation.**

I. INTRODUCTION

MULTILEVEL inverter technology has been widely used for the control of medium- and high-voltage ac drive applications from the past few decades because of its improved output voltage quality, better harmonic performance, less voltage stress on power electronic devices, and so on. The basic concept of multilevel inverters is to achieve the staircase voltage waveform by using more low-rated power electronic switches and voltage sources. As the number of out-put voltage levels increase, the requirement of series-connected switches will also increase in the case of conventional multilevel inverters such as diode clamped and flying-capacitor (FC) multilevel inverters. Therefore, if any of the switches fails, the entire topology has to be shut down resulting in decreased system reliability. Moreover, these topologies have some inherent drawbacks such as neutral-point voltage balancing and capacitor voltage balancing problems, which in turn cause unequal voltage sharing across the switches and adds dc offset voltage to the output voltage waveform.

Therefore, special capacitor voltage balancing techniques are needed to eliminate these issues. The reliability of the system can be increased using the H-bridge configuration, as presented in, which will also eliminate the capacitor voltage balancing issue and the neutral-point voltage balancing issue.

However, as the number of voltage levels increase, it requires more isolated dc sources. Another interesting topology to increase the reliability of The system is the dual-inverter configuration using an open-end winding induction motor. In this configuration, the neutral point
Of the induction motor is disconnected, and both sides of the winding are fed from two two-level (or multilevel) inverters. This configuration requires only half of the dc source voltage when compared with conventional neutral-point-clamped (NPC) or FC multilevel inverters. To eliminate the aforementioned problems, such as capacitor voltage balancing and the requirement of more voltage sources, a five-level inverter topology is presented in, which uses three dc sources to obtain a five-level voltage waveform. In this paper, the advantage of two IVPWCs of a four pole induction motor is used in designing the multilevel inverter Topology.

On the other hand, an open-end winding induction motor supplied by SVPWM-controlled multilevel inverters with a single dc source will provide path for the zero-sequence currents, because of the dominant lower order harmonic voltages in the inverter output voltage. A five-level inverter topology for a four-pole induction-motor drive with a single dc link is presented in, which has used SPWM to minimize the zero-sequence currents though the motor

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ISSN (Online) 2395-2717
International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
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phase windings. However, this scheme is effective in the linear modulation only.

II. VOLTAGE EQUATIONS OF INDUCTIONMOTOR STATOR WINDING

It is well known that, in a conventional ac machine, the winding coils which are 360
◦ (electrical) apart will have identical voltage profiles across them. Thus, the four-pole induction motor consists of two IVPWCs (where the number of IVPWCs is equal to the number of pole pairs). In the conventional four-pole induction motor, these two windings are connected in series, as shown in Fig. 1(a). However, in this paper, these are disconnected, as shown in Fig. 1(b). As the two windings are disconnected exactly with an equal number of turns, it can be written [as shown in Fig. 1(a) and (b)] as

N1=N2=N⁄2 (1)

Reluctance is given by =1⁄**μA** (2)

The following observations can be made when compared withconventional-induction-motor parameters.
a) Stator resistance (*rs* = *ρl/A*) will be half because the length of the copper is half.
b) Reluctance offered to the leakage flux will be half because the mean length of the stator leakage flux is hal ; hence, from (1) and (2), the leakage inductance (***L1ls*** = **N1**^{2}/) will be half. c) Reluctance offered to the magnetizing flux will be the same because the mean length of the core is the same in both cases. Therefore, from (1) and (2), the magnetizing inductance (***Lms*** = *N1N2/*) will be 1/4 times.
From the above discussion and by writing KVL shown in Fig. 1(b), the voltage across one IVPWC of A-phase can be obtained as

$$va1-va2=\frac{rs}{2}ias+\frac{Lss}{2}pias-\frac{1}{2}\frac{Lm}{2}pibs-\frac{1}{2}\frac{Lm}{2}pics \quad (3)$$

The voltage across the other IVPWC of A-phase can be obtained by writing Kirchhoff's voltage law (KVL) shown in

Fig. 1(b), i.e.,

$$va3-va4=\frac{rs}{2}ias+\frac{Lss}{2}pias-\frac{1}{2}\frac{Lm}{2}pibs-\frac{1}{2}\frac{Lm}{2}pics \quad (4)$$

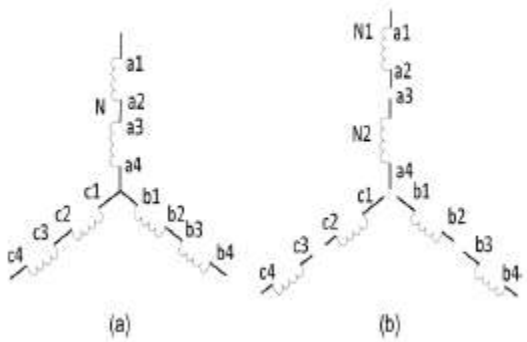

Fig. 1.Induction motor stator winding. (a) General arrangement. (b) Arrangement for the proposed inverter.

The effective voltage across the stator winding is the sum of the voltages across the two individual windings, i.e.,

$$V_{as}=(V_{a1}-V_{a2})+(V_{a3}-V_{a4}). \quad (5)$$

The motor phase voltage can be achieved by substituting (3) and (4) into (5) as follows:

$$Vas=RsIas+LssPias-\frac{1}{2}LmpPIbs-\frac{1}{2}LmPIcs \quad (6)$$

The voltage across the total winding of A-phase can be obtained by writing the KVL shown in Fig. 1(a), which is equal to the (6). It can be observed from the above discussion that (6) and the voltage equation of the conventional induction motor presented in [22] are identical.

III. PROPOSED MULTILEVEL INVERTER TOPOLOGY

The five-level inverter topology uses three dc sources to obtain a five-level voltage waveform. Mostly diode bridge rectifiers are used for providing dc supply. There-fore, in regenerative braking, it requires three braking rheostats and three control mechanisms to protect the rectifier units, which complicate control and power circuits. In this paper, three dc sources are replaced by a single dc source, as shown in Fig. 2.

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ISSN (Online) 2395-2717
International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
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The two disconnected IVPWCs are supplied with four conventional two-level inverters, and all of them are connected to the same dc source, as shown in Fig. 2. The maximum voltage blocking capacity of all two-level inverter switches is equal to input dc source voltage (*vdc*/4). Two switches in the same leg of the two-level inverters complement each other. S***1*** to S***6*** are bidirectional (four quadrant) switches that can allow the current in both directions and can block the voltage in both directions. The maximum voltage blocking capacity of these switches is *vdc*/8 only. All these (main and auxiliary) switches are switched in such a way that it produces five-level voltage ((*vdc*/2), (*vdc*/4), 0, (−*vdc*/4), (−*vdc*/2)) across the motor phase winding, and the possible switching combinations are shown in Table I. Permanent shorting of the bidirectional switches cause unequal voltages across IVPWCs during some ((−*vdc*/4), 0, (*vdc*/4)) voltagelevel synthesis. Hence, control of these bidirectional switches is important, which is explained.

The proposed multilevel inverter topology is compared with the conventional five-level NPC inverter, FC inverter, and

Table I Possible Switching Combinations To Generate Five-Level Voltage Waveforms

Voltage Magnitude	S_{11}	S_{21}	S_{31}	S_{41}	S_1	S_2
$+\frac{V_{dc}}{2}$	ON	OFF	ON	OFF	ON	ON
$+\frac{V_{dc}}{4}$	ON	ON	ON	OFF	OFF	OFF
	ON	OFF	OFF	OFF	OFF	OFF
0	OFF	OFF	OFF	OFF	OFF	OFF
	ON	OFF	OFF	ON	OFF	OFF
	ON	ON	ON	ON	OFF	OFF
	OFF	ON	ON	OFF	OFF	OFF
$-\frac{V_{dc}}{4}$	OFF	OFF	OFF	ON	OFF	OFF
	OFF	ON	ON	ON	OFF	OFF
$-\frac{V_{dc}}{2}$	OFF	ON	OFF	ON	ON	ON

H-bridge inverter, as shown in Table II. The proposed topology is free from neutral-point voltage balancing issues because the clamping diodes are not used unlike in the diode clamped topologies. The capacitor voltage balancing issues are also eliminated because it does not require any capacitor banks unlike FC inverters. Only a single dc source is used in this configuration; therefore, power balancing issues and issues in regenerating mode are minimized. The magnitude of the dc bus requirement is also less (*vdc*/4).

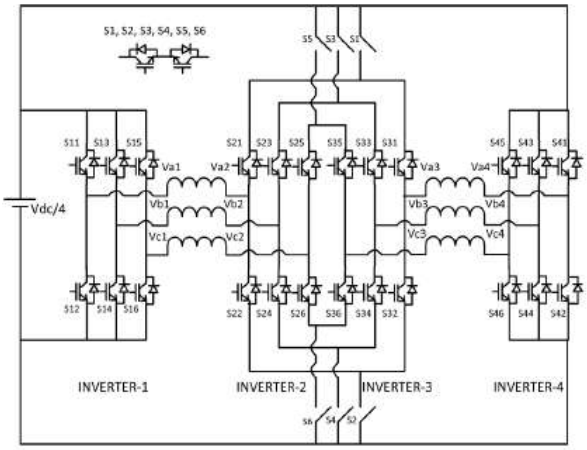

Fig. 2. Proposed multilevel inverter topology

IV. SPWM

A. Linear Modulation Region (0 < mi < 1)

Gating pulses for the proposed multilevel inverter are generated using SPWM with a real-time digital simulator. Three modulating signals (sine waves) and four carrier signals

Table II Comparison between the Conventional Topologies with the Proposed Topology

	NPC	FC	H-bridge inverter	Proposed Topology
Main switches	24	24	24	24
Clamping Diodes	36	0	0	0
Isolated voltage sources	1 (V_{dc})	1 (V_{dc})	6 ($\frac{V_{dc}}{4}$)	1 ($\frac{V_{dc}}{4}$)
Capacitors Banks	4	18	0	0
Bi-directional switches	0	0	0	6 ($\frac{V_{dc}}{8}$)

(Triangular waves) are used to produce the gating pulses for the proposed topology, as shown in the Fig. 3. The maximum frequency of the modulating signal (sine wave) is 50 Hz; however, carrier signal frequency is kept constant at 2 kHz. Many switching combinations are possible (which are shown in Table I), but the switching combinations shown in Table III give less switching transitions from one voltage level to another. The remaining

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ISSN (Online) 2395-2717
International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
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switching combinations (in Table I) are used in the case of fault condition, to increase the reliability of the system. In the case of any switch failure of the middle two inverters (inverters 2 and 3), the entire system need not to be shut down. Instead, it can be operated as a three-level inverter up to a modulation index of 0.5 (where modulation index is equal to the ratio of the peak of the modulating signal to four times the peak of the carrier signal, as shown in Fig. 3). For example, when switch S***21*** is open (or S***22*** is shorted), the possible switching combinations

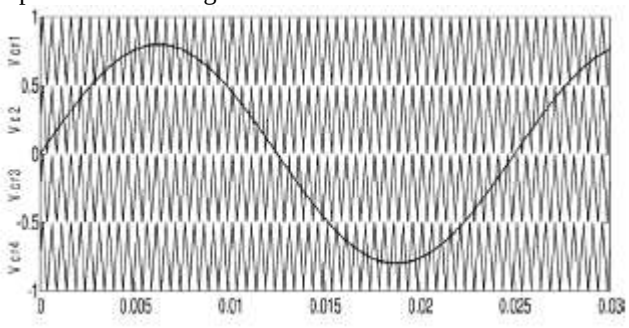

Fig. 3. Modulating and carrier waves for generating gating pulses in SPWM are shown in Table IV.

Table III Comparison of carrier and modulating signals Corresponding to the output voltage

Comparison between Modulating and Carrier signals	Output Voltage Level	Optimum switching combinations
$V_M > V_{cr1}$	$+\frac{V_{dc}}{2}$	S_{11}, S_{22}, S_{31}, S_{42} S_1 and S_2
$V_{cr2} < V_M < V_{cr1}$	$+\frac{V_{dc}}{4}$	S_{11}, S_{22}, S_{32} and S_{42}
$V_{cr3} < V_M < V_{cr2}$	0	S_{12}, S_{22}, S_{32} and S_{42}
$V_{cr4} < V_M < V_{cr3}$	$-\frac{V_{dc}}{4}$	S_{12}, S_{22}, S_{32} and S_{41}
$V_M < V_{cr4}$	$-\frac{V_{dc}}{2}$	S_{12}, S_{21}, S_{32}, S_{41}, S_1 and S_2

Table IV
Possible Switching Combinations During Fault Condition

Voltage Magnitude	S_{11}	S_{21}	S_{31}	S_{41}	S_1	S_2
$-\frac{V_{dc}}{4}$	ON	OFF	OFF	OFF	OFF	OFF
0	OFF	OFF	OFF	OFF	OFF	OFF
$-\frac{V_{dc}}{4}$	OFF	OFF	OFF	ON	OFF	OFF

B. Over modulation (mi > 1)

The linear modulation region can be significantly increased by adding the zero-sequence component to the modulating signals in SVPWM [24]. Due to the addition of the zero sequence component, the sum of instantaneous reference phase signals are not equal to zero (***Va*** + ***Vb*** + ***Vc*** = 0), which can produce lower order zero-sequence currents in the motor phase windings. Therefore, the SVPWM technique is not best suitable for those configurations that provide a closed path for zero-sequence currents (generally, open-end winding induction-motor drives with a single dc link) [19]. In this paper, a modified SPWM technique is proposed to operate the configuration in the over modulation region. In this technique, whenever an A-phase modulating signal is crossing the peak of the upper carrier signal ***Vtp***, it is clamped to***Vtp***. The subtracted magnitude of the A-phase signal (i.e., ***Va*** – ***Vtp*** shown in Fig. 4) is proportionally added to B-phase and Cphase modulating signals such that the sum of the three phase modulating signals equal to zero (***Va*** + ***Vb*** + ***Vc*** = 0). Hence, the magnitude added to the B-phase is given by ***Vb***(***Va*** – ***Vtp***)/***Va***, and that to the C-phase is given by ***Vc***(***Va*** – ***Vtp***)/***Va***, as shown in Fig. 4. The same procedure is followed for the B-phase and the C-phase. It is well known that when the modulation index is varying between 1 to 2/√3, the maximum of one phase modulating

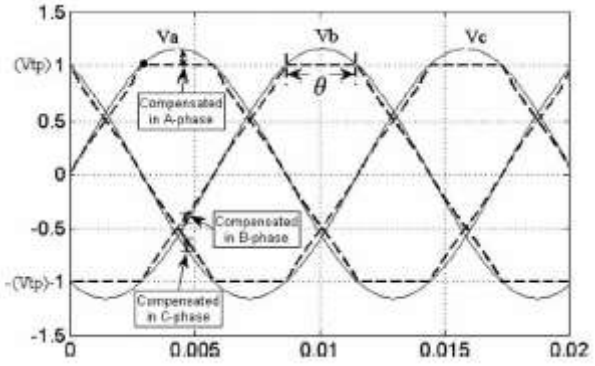

Fig.4.Three phase modulating waves in over modulation after compensation.

Signal crosses the peak of the upper carrier signal, and for a modulation index greater than 2/ √3, the maximum of two or three phase modulating signals cross the peak of the carrier signal simultaneously. Therefore, using the proposed method, it is possible to operate the drive in the over modulation region up to the modulation index of 2/ √3. Beyond this modulation index, as two modulating signals are crossing the peak of the carrier wave simultaneously, it results to the considerable reduction in the fundamental component.

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ISSN (Online) 2395-2717
International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
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The line-to-line modulating signals are shown in Fig. 5 for different modulation indexes to demonstrate the maximum possible limit of the modulation index. It is clearly shown in

Fig. 5(a) and (b)

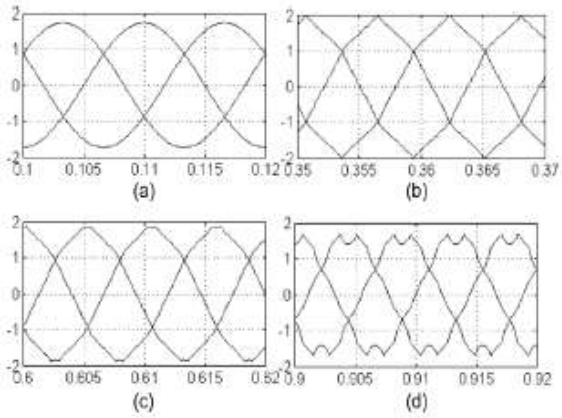

Fig.5. Three phase line to-line modulating waves in over modulation after compensation. (a) mi = 1, (b) mi = 1.15, (c) mi = 1.25, and (d) mi = 1.5.

That the fundamental voltage magnitude is increasing from the modulation index of 1 to 2/√3 and it starts decreasing from2/√3, as shown in Fig. 5(c) and (d).
In the proposed method, the average value of the line-to line modulating signal is calculated by assuming ***Vtp*** = 1. The expression for the line-to-line modulating signal is written from Fig. 4 (dotted lines) and integrated from $\pi/3$ to $5\pi/6$ (since the waveform is following quarter-wave symmetry, any 90° duration can be considered) to get the average value; this is given in (7), shown at the bottom of the next page, where The expression for the line-to-line modulating signal in conventional SPWM over modulation is also written from Fig. 4 (solid lines) and integrated from $\pi/3$ to $5\pi/6$ swoll of as

$$Vab=\frac{2}{\Pi}\left\{\int_{\frac{\Pi}{3}}^{\frac{\Pi}{2}-\frac{\theta}{2}}\left(VmSin(wt)-VmSin\left(wt-\frac{2\Pi}{3}\right)\right)dwt\right.$$
$$+\int_{\frac{\Pi}{2}-\frac{\theta}{2}}^{\frac{\Pi}{2}+\frac{\theta}{2}}\left(1-VmSin\left(wt-\frac{2\Pi}{3}\right)\right)dwt$$
$$+\int_{\frac{\Pi}{2}+\frac{\theta}{2}}^{\frac{5\Pi}{6}-\frac{\theta}{2}}\left(VmSin\left(wt\right)-VmSin\left(wt-\frac{2\Pi}{3}\right)\right)dwt$$
$$\left.+\int_{\frac{5\Pi}{6}-\frac{\theta}{2}}^{\frac{5\Pi}{6}}\left(VmSin\left(wt\right)-VmSin\left(wt-\frac{2\Pi}{3}\right)\right)dwt\right\} \quad (8)$$

The point to be noticed is that, whenever the peak of the modulating signal is crossing ***Vtp***, it should be clamped to ***Vtp*** Therefore, the reduction in the line-to-line modulating signal of the proposed method when compared with conventional over modulation is given by.

$$Vab-Vab1=\left(\frac{2}{\Pi}\right)\left(\begin{array}{l}VmSin\left(\frac{\theta}{2}\right)-\left(\frac{\theta}{2}\right)\\+3\left[VmCos\left(\frac{\theta}{2}\right)-\ln\left(\cos\left(\frac{\theta}{2}\right)\right)-Vm\right]\end{array}\right) \quad (9)$$

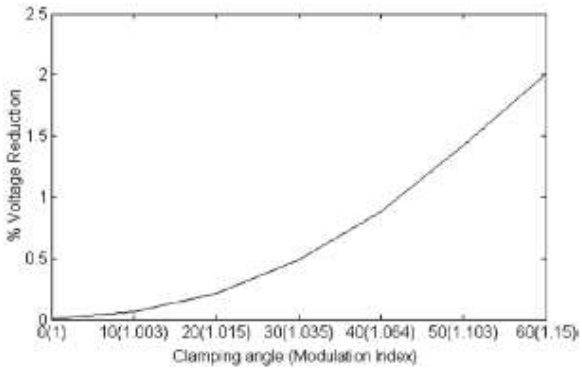

Fig. 6. Percentage magnitude reduction of the line-to-line modulating signal with respect to the modulation index

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ISSN (Online) 2395-2717
International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
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Where

$$Vm = \frac{1}{\sin\left(\frac{\Pi}{2} - \frac{\theta}{2}\right)}$$

The percentage reduction in the line-to-line modulating signal is calculated, and it is plotted for different Modulation indexes, as shown in Fig. 6. It can be noticed in Fig. 6 that the loss in line-to-line voltage is at the maximum of 2%, which is negligible.

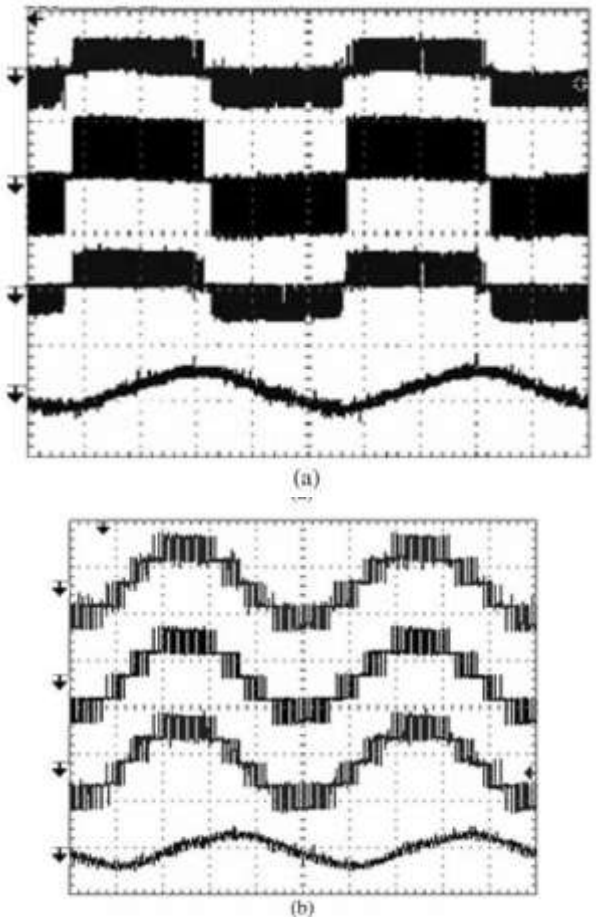

Fig. 7. Top trace is the voltage across the first winding

(***Va1*** − ***Va2***), the second trace is the effective voltage across the total stator phase winding, the third trace is the voltage across the second winding (***Va3*** − ***Va4***), and the bottom trace is the stator current (*Ia*) for the modulation index of (a) 0.4 [*y*-axis 100 V/div, 2 A/div; *x*-axis 10 ms/div] and (b) 0.8 [*y*-axis 100 V/div (for first and third from top), 200 V/div (for second from top), 2 A/div; *x*-axis 5 ms/div].

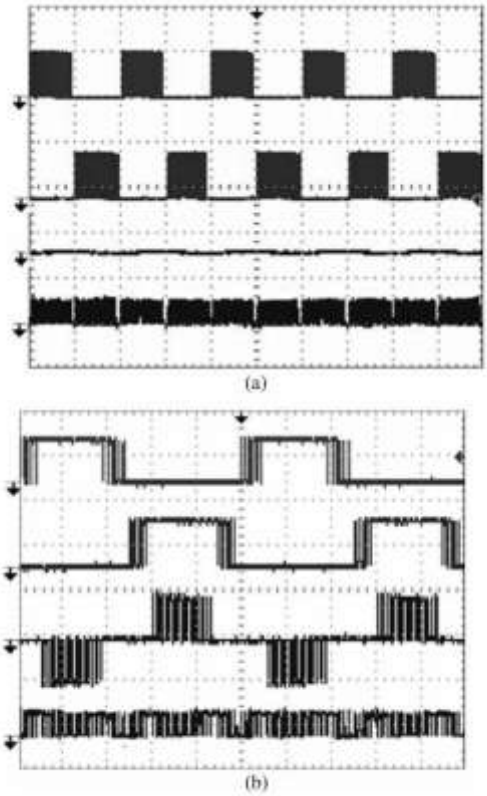

Fig. 8. Top trace is the inverter-1 pole voltage

the second trace is the inverter- 4 pole voltage, the third trace is the voltage between the middle two inverters, and the bottom trace is the voltage across bidirectional switch for the modulation index of (a) 0.4 [*y*-axis 100 V/div; *x*-axis 25 ms/div] and (b) 0.8 [*y*-axis 100 V/div; *x*-axis 5 ms/div].

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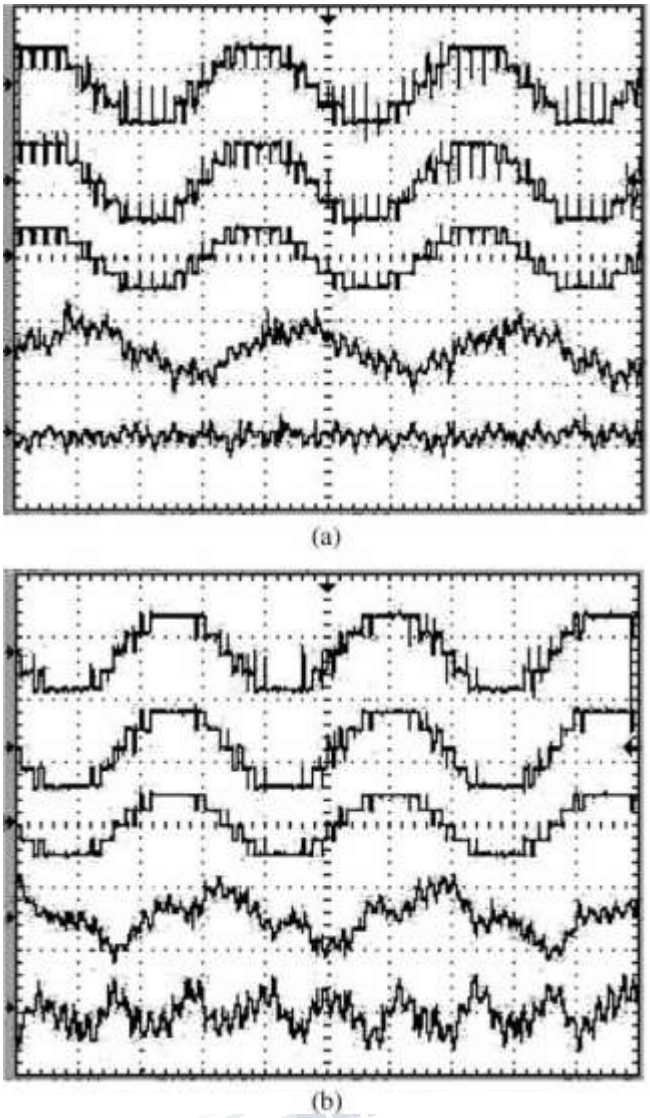

Fig. 9. Top trace is the voltage across the first winding

(***Va1*** − ***Va2***), the second trace is the effective voltage across the total stator phase winding, the third trace is the voltage across the second winding (***Va3*** − ***Va4***), the fourth trace is the stator current (***Ia***), and bottom trace is the zero-sequence currents for the modulation index of ***2/√3***. (a) Proposed method [*y*-axis (200 V/div, 500 V/div, 2 A/div, *x*-axis 5 ms/div]. (b) Conventional SPWM [*y*-axis (200 V/div, 500 V/div, 2 A/div, *x*-axis 5 ms/div].

VI. CONCLUSION

In this paper, a multilevel inverter topology has been presented for a four-pole induction-motor drive. The disconnected two IVPWCs are fed from four two-level inverters. All these four two-level inverters are connected to a single dc source minimizing the power balancing issues. The magnitude of dc source voltage requirement is also very less compared with that of conventional five-level inverter topologies. This topology uses only two-level inverters; hence, it is free from capacitor voltage balancing issues. The proposed topology is experimentally verified with a 5-hp four-pole induction motor using a laboratory prototype. Gating pulses are generated using the SPWM technique for the linear modulation region and for the over modulation region using the modified SPWM technique. In the case of any switch failure of the middle two inverters, the topology can be operated as a three-level inverter up to the modulation index of 0.5. This will increase the reliability of the system during fault condition when compared with conventional NPC or FC topologies. This topology does not require any major design modifications of the induction motor except the disconnection of IVPWCs. This concept can also be applied to obtain a higher number of voltage levels for the induction motor with a higher number of poles, which requires more two-level inverters.

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