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An Asymmetric Multilevel Inverter Topology for PV Applications with Reduced Number of Power Electronic Components

[1] K.Srinivasu [2] S.M.Shariff [3] Dr. K.Satyanarayana
[1] M.Tech Scholar [2] Associate Professor, [3] Professor & HOD
Department of Electrical & Electronics Engineering,
Pragati Engineering College, A.P, India

***Abstract:*--Multilevel inverter performance is high compared to the conventional two level inverters due to their reduced harmonic distortion, lower electromagnetic interference. However the main drawback of multilevel inverter is increased number of switches, complex pulse width modulation control and balancing of capacitor voltages. This paper proposes a single phase fifteen level inverter for photo-voltaic applications. The proposed inverter topology consists of fewer components with low complexity gate drives and control signals. This paper also presents the most relevant control and modulation methods like Staircase modulation technique with sinusoidal wave as reference.**

In this paper also studied proposed multilevel inverter topology for both symmetric and asymmetric configurations. Proposed multilevel inverter is compared with already existing inverter topologies. The entire system is numerically simulated using MATLAB/SIMULINK and the simulation results are presented.

***Keywords*—Symmetric Multilevel inverter, Asymmetric Multilevel inverter, THD, PV Cell**

I. INTRODUCTION

Multilevel power conversion was first introduced more than twenty years ago. Multilevel inverters are becoming recent trends, because of its modularity and simplicity of control to generate particular number of levels. Multilevel inverters have a number of applications such as ups, in power grid, as solar inverter, induction heating and number of other applications. The multilevel inverter has drawn tremendous interest in the power in the power industry [2]. By using multilevel inverter to produce quality output voltage or a current waveform with minimum amount of ripple content [3]. It can be possible by using more number of active semiconductor switches to perform conversion in small voltages steps. One area where multilevel converters are mostly suitable is that of renewable photovoltaic energy that efficiency and power quality are of concerns for the researchers. Multilevel inverter mostly popular area where the numbers of switches are reduced. A sine wave output is desirable because many electrical products are engineered to work best with a sine wave ac power source. The standard electric utility power attempts to provide a power source that is a good approximation of a sine wave.Switch mode power supply (SMPS) devices, such as personal computers function on quality of sine wave power. Ac motors directly operated on non-sinusoidal power may produce extra heat, may have different speed-torque characteristics, or may produce more audible noise than when running on sinusoidal power thus the multilevel inverters with reduced number of switches becomes more significant.

1.1. Conventional Systems

The multilevel inverters are classified as, neutral point clamped inverters, flying capacitor multilevel inverters and cascade multilevel inverters. Conventional multi-level inverters, such as diode clamped multi-level inverters, flying capacitor multi-level inverters and CMLIs have some drawbacks if the number of voltage levels increases, the cost of the switching components and capacitors increases quickly as the number of voltage levels grows, and it also happens to the complexity of their implementations. Out of these three categories cascaded multilevel inverter is recent trend because of its reliability. Table III & IV shows the comparison of conventional multilevel inverters switching components.

II. CASCADED MULTILEVEL INVERTER TOPOLOGY

Cascaded multilevel inverters can be classified as symmetric and asymmetric multilevel inverters. The main difference between symmetric and asymmetric configuration

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is the magnitude of dc sources. By using the cascaded multilevel inverters desired number of output voltage levels can be obtained by series connection of a number of dc voltage sources.

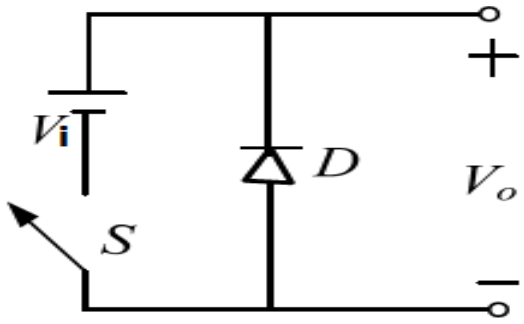

Fig 2.1: Basic Unit for a Sub-Multilevel Converter

The selected cascaded multilevel inverter topology uses series connected sub multilevel converters. Fig. 2.1 shows the basic unit for a sub multilevel converter.

This topology of inverter uses sub multilevel inverter part and polarity creator. The sub multilevel converter gives either zero or positive . The sub multilevel converter can be operated in eighter symmetrical or asymmetrical mode depending on the following equations. When

$V_i = V_{dc}$ →Symmetrical Multilevel Inverter

$V_i=2^{(i-1)} V_{dc}$ or 3^iVdc →Asymmetrical Multilevel Inverter

Where i=1, 2,3,4,…… n [8]

III.PROPOSED INVERTER TOPOLOGY

Proposed multilevel inverter is a combination of sub multilevel converters. It is divided into two main parts first one is a level generator for generating required level of output and second part is polarity creator for generating positive and negative levels at output. Fig 3.1 shows the proposed inverter topology.

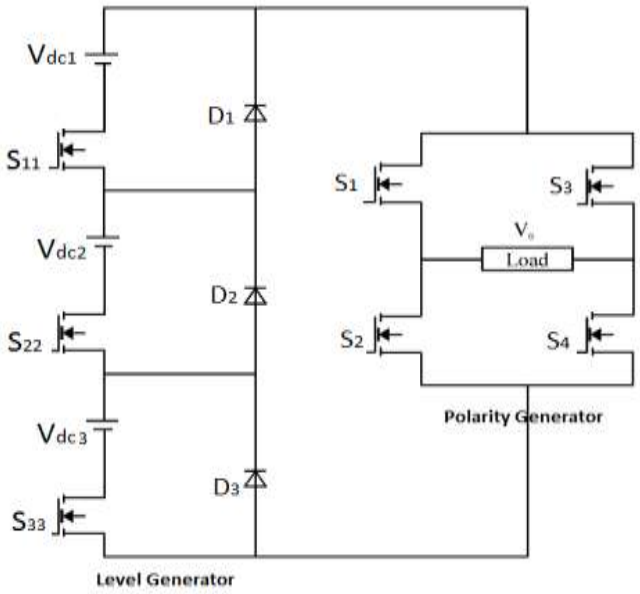

Fig.3.1 Proposed multilevel inverter topology

IV. CIRCUIT DESCRIPTION

In conventional multilevel inverters, the power semiconductor switches are combined to produce a high-frequency waveform in positive and negative polarities. However, there is no need to utilize all the switches for generating bipolar levels. This idea has been put into practice by the new topology. This topology is a hybrid multilevel topology which separates the output voltage into two parts. One part is named level generation part and is responsible for level generating in positive polarity. This part requires high-frequency switches to generate the required levels. The switches in this part should have high-switching-frequency capability. The other part is called polarity generation part and is responsible for generating the polarity of the output voltage, which is the low-frequency part operating at line frequency. The topology combines the two parts (high frequency and low frequency) to generate the multilevel voltage output. In order to generate a complete multilevel output, the positive levels are generated by the high-frequency part (level generation), and then, this part is fed to a full-bridge inverter (polarity generation), which will generate the required polarity for the output. This will eliminate many of the semiconductor switches which were responsible to generate the output voltage levels in positive and negative polarities.

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V. POWER STAGE OPERATION FOR ASYMMETRIC CONFIGURATION

In the simulation Vpu= 25V is considered so the value of the three dc sources are 25V ,50V and 100V as per the equation. With the given magnitude of dc voltage source the Fifteen voltage levels are generated by the combination of the switches for the proposed inverter topology shown in fig.3.1.

TABLE-I
Switching Combination Required To Generate Each Output Voltage Level

Output Voltage	Switching States						
	S_{33}	S_{22}	S_{11}	D_3	D_2	D_1	Level
0V	0	0	0	1	1	1	1
25V	0	0	1	1	1	0	2
50V	0	1	0	1	0	1	3
75V	0	1	1	1	0	0	4
100V	1	0	0	0	1	1	5
125V	1	0	1	0	1	0	6
150V	1	1	0	0	0	1	7
175V	1	1	1	0	0	0	8

Power Stage Operation For Symmetric Configuration

In the simulation Vpu= 50V is considered so the value of the three dc sources are 50V ,50V and 50V as per the equation.With the given magnitude of dc voltage source the Seven voltage levels are generated by the combination of the switches for the proposed inverter topology shown in fig.3.1.

TABLE-II
Switching Combination Required To Generate Each Output Voltage Level

Output Voltage	Switching States						
	S_{33}	S_{22}	S_{11}	D_3	D_2	D_1	Level
0V	0	0	0	1	1	1	1
50V	0	0	1	1	1	0	2
100V	0	1	1	1	0	0	3
150V	1	1	1	0	0	0	4

Number of Components Required

One of the important advantages of the proposed topology is that it requires less number of high-switching frequency power semiconductor components. Thus the reliability of the converter is increased. It can be clearly seen that the number of components of the power stage is lower than that of other topologies like the diode clamped and the neutral point clamped configurations, and a new and highly improved multilevel stage. Table III & Table IV shows the comparison of number of components required for different Fifteen level & Seven level inverter topologies[10].

TABLE-III
Number Of Components Required For Single Phase Fifteen-Level Inverter Topologies

MLI Type	Diode Clamped	Flying Capacitor	Cascaded H-Bridge	Proposed Asymmetric Topology
Main Switches	28	28	28	7
Clamping & anti-parallel Diodes	210	28	28	10
Capacitors	14	105	7	0
Sources	1	1	7	3
Total Number	253	162	70	20

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TABLE-IV
Number Of Components Required For Single Phase Seven-Level Inverter Topologies

MLI Type	Diode Clamped	Flying Capacitor	Cascaded H-Bridge	Proposed Symmetric Topology
Main Switches	12	12	12	7
Clamping & anti-parallel Diodes	24	12	12	10
Capacitors	3	9	3	0
Sources	1	1	3	3
Total Number	40	34	30	20

IV. MULTILEVEL PWM MODULATION

The modulation schemes for CMLIs are mostly based on multiple-carrier arrangements with PWM. Therefore, in the traditional PWM scheme, the N voltage levels need N carrier signals that are arranged with vertical shifts or horizontal displacements. As a result, the high-order harmonic components generated by the PWM scheme can be attenuated easily by filter or load inductance, hence providing an output voltage with good reference tracking and low harmonic distortion. However, it also leads to high switching losses as the device switching frequency is usually quite high. At the same time, N carrier signals make the implementation very complicated. As a result, staircase modulation [13] with low device switching frequency is introduced. Fig.4.1 shows the stepped-voltage waveform consisting of the output of the 3-H-bridge modules with switching angles of triggering signals. The switches are switched at very low frequency and the inverter is driven by the fundamental switching strategy leads to low electromagnetic interference (EMI). It consists of eight switching angles(θ_1 to θ_8) at which each level is generated and the switches are switched.

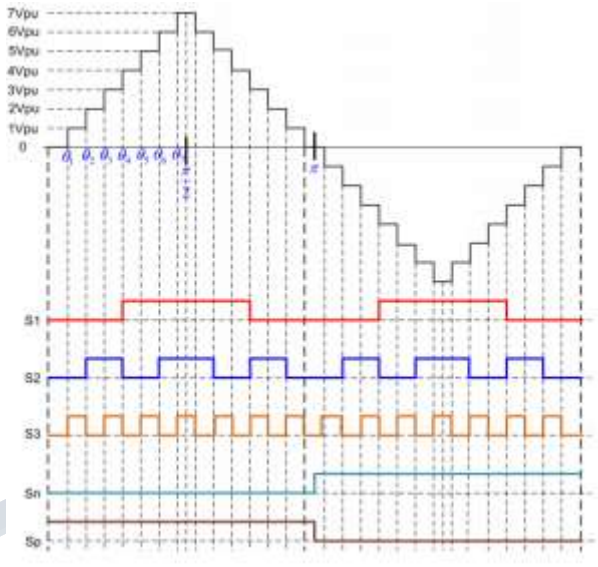

Fig. 4.1: Stepped-voltage waveform consists of the output of level generator with switching angles for IGBTs

The switching frequency of this circuit can be given by:

$$f\_switch = f\_fundamental \times 2(2^n - 1)$$

Where the fundamental frequency is 50Hz, n represents the number of the particular H-bridge in per unit voltage order. The H-bridge with higher voltage output works at a lower switching frequency comparing to the H-bridge with lower voltage output, which reduces the switching losses largely.

The reference sine wave is having maximum amplitude of 1 and is divided into seven steps of equal magnitude equal to 1 / 8 = 0.125. Each step corresponding to switching angle for particular switch.

The logic functions for the gate signals are generated as follows. Reference sine wave after taking its absolute value is termed as V_{ref} and before taking absolute is termed as V_r. In this paper sine wave as a reference wave by connecting absolute sine wave is taken and from this gating signals are generated and then we can trigger the IGBTs.

V. MODELLING OF SOLAR CELL

A solar cell is the building block of a solar panel. A photovoltaic module is formed by connecting many solar cells in series and parallel. Considering only a single solar cell; it can be modeled by utilizing a current source, a diode and two

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resistors. This model is known as a single diode model of solar cell [12].

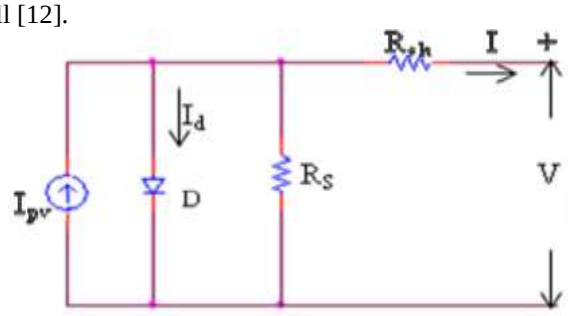

Fig. 5.1. single diode model of solar cell

The characteristic equations for a photovoltaic cell are given as follows:

Open circuit voltage of solar cell: $Voc = (AKT_c/q)\ ln\ (I_{pv}/I_s)$ Output current of solar cell is given by $I= I_{pv}-I_d-I_{sh}$

$$I= I_{pv}-I_s\exp[((q/AKT_cN_s)v+IR_s)-1]-(V+IR_s)/R_{sh}$$

Where, Ns is number of cells in series for a PV module.

The light generated current of the solar cell is mainly depends on the solar irradiation level and its working temperature, which is expressed as

$$I_{pv}=[I_{sc}+K_I(T_c-T_r)]G$$

Where, I_{sc} is the short-circuit current of cell at 25°C and 1000W/m^2, K_I is the short-circuit current temperature co-efficient of cell, Tc and Tr are the working temperature of cell and reference temperature respectively in ^oK.

The diode saturation current of the cell varies with the cell temperature, which is expressed as

$$I_s = I_{rs}\ (T_c/T_r)^3\ \exp[qEg/AK(1/T_c - 1/T_r)$$

Where, I_{rs} is the reverse saturation current of a cell at a reference temperature and a solar irradiation, Eg is the band gap energy of the semiconductor used in the cell (Eg ≈1.12 eV for the polycrystalline Si) at 25 ^oC.

The reverse saturation current of a cell I_{rs} is

$$I_{rs} = I_{sc}\ /[\exp[(q/AKT_cN_s)V_{oc}]-1]$$

VI. SIMULATION RESULTS

In order to verify the proposed inverter topology and the switching pattern, simulations are performed by using MATLAB/SIMULINK

The waveforms of the seven level Symmetric multilevel inverter with R- Load and a series R-L load of 150Ω and 30mH respectively are shown in Figures.

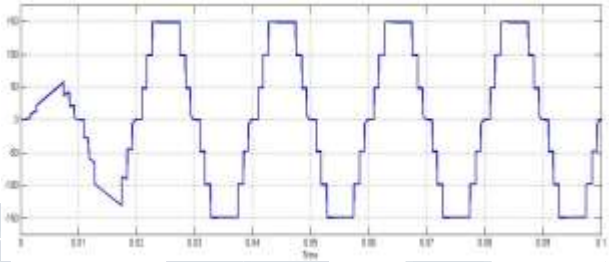

Fig.6.1. Output voltage of Symmetric Seven level inverter with R(150Ω)Load

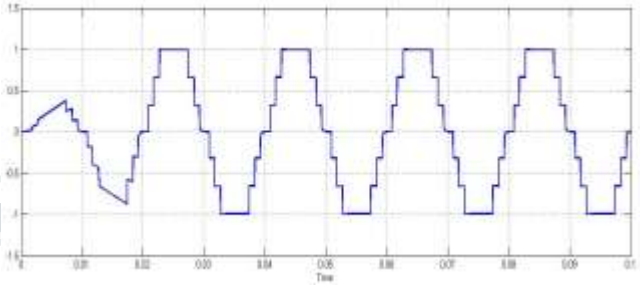

Fig.6.2. Output current of Symmetric Seven level inverter with R(150Ω)Load

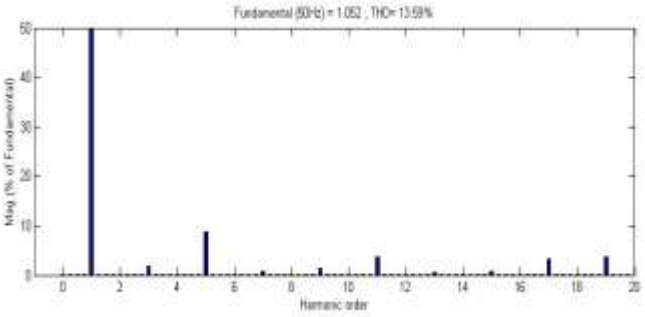

Fig.6.3. Output current THD Symmetric Seven level inverter with R- Load

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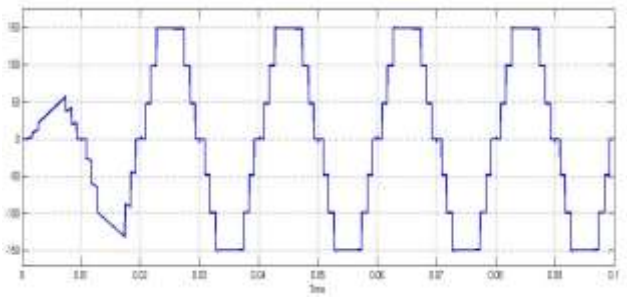

Fig.6.4. Output voltage of Symmetric Seven level inverter with RL(150 Ω,30mH)- Load

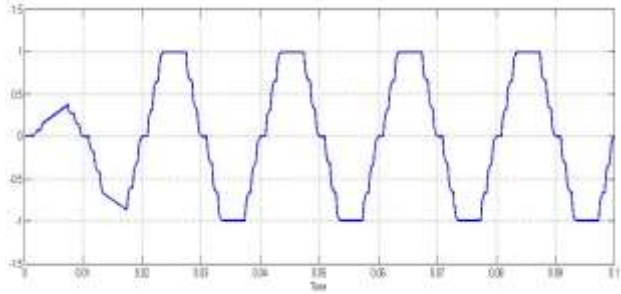

Fig.6.5. Output current of Symmetric Seven level inverter with RL(150 Ω,30mH)- Load

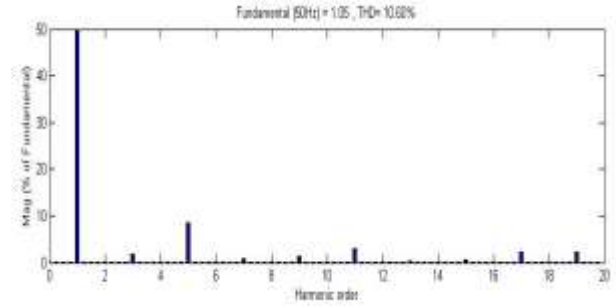

Fig.6.6. Output current THD Symmetric Seven level inverter with RL- Load

The waveforms of the Fifteen level Asymmetric multilevel inverter with R- Load and a series R-L load of 150Ω and 30mH respectively are shown in Figures.

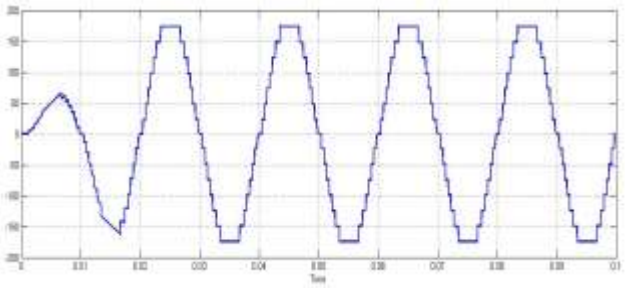

Fig.6.7. Output voltage of Asymmetric Fifteen level inverter with R(150Ω)Load

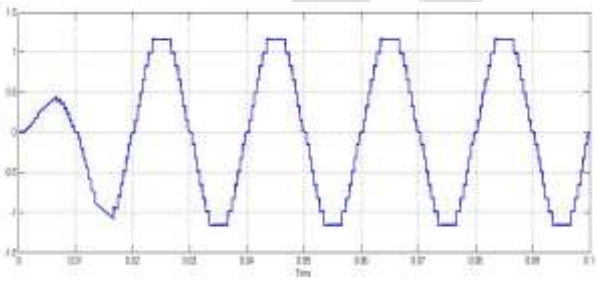

Fig.6.8. Output current of Asymmetric Fifteen level inverter with R(150Ω)Load

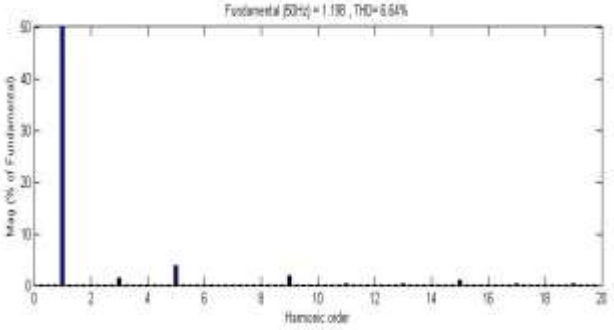

Fig.6.9. Output current THD Asymmetric Fifteen level inverter with R- Load

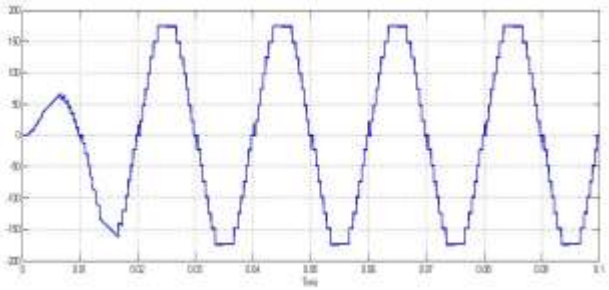

Fig.6.10. Output voltage of Asymmetric Fifteen level inverter with RL(150 Ω,30mH)- Load

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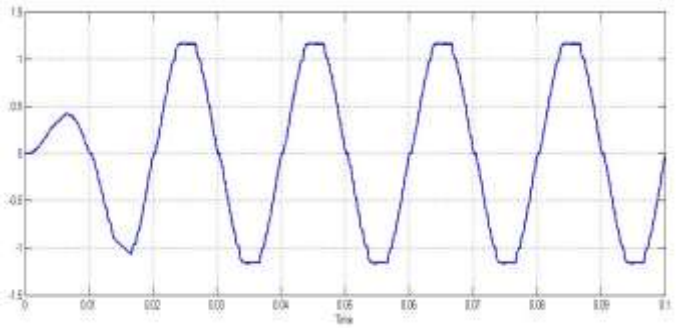

Fig.6.11. Output current of Asymmetric Fifteen level inverter with RL(150 Ω,30mH)- Load

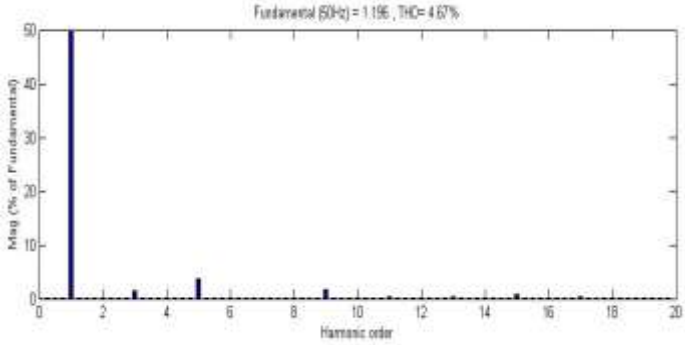

Fig.6.12. Output current THD Asymmetric Fifteen level inverter with RL- Load

Table V Shows THD comparison of symmetric and asymmetric configurations of proposed topology without any filter.

TABLE V THD Comparison

MLI Type	Voltage THD %		Current THD%	
	R-Load	RL-Load	R-Load	RL-Load
Symmetric 7 Level Inverter	13.59	13.92	13.59	10.60
Asymmetric 15 Level Inverter	6.64	6.80	6.64	4.67

VII. CONCLUSION

In this paper a new inverter topology which has superior performance, offering improved output waveforms and lower THD over conventional topology in terms of number of switches required, cost, control system and reliability. The number of power semiconductor switches required for the proposed inverter is very less in number which reduces switching losses and thereby increasing efficiency of the inverter. Proposed topology is studied in both symmetric and asymmetric configurations with Resistive and Inductive loads and these are operated from solar power. Obtained results are satisfactory with reduced THD content in the output and it is best suitable for PV applications. Also the operating principles and the switching functions are analyzed. The complexity of switching for this topology is low. The results obtained clearly shows the effectiveness of the proposed topology as an asymmetric fifteen level inverter compared to symmetric seven level with reduced number of switches. This proposed multilevel inverter Topology can be extended for higher number of levels with few number of changes made in proposed topology.

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