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# Design, Modelling and Analysis of Two Phase Interleaved Buck DC-DC Converter

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***Abstract:*** **-- The two phase interleaved buck converter (IBC) for low input voltage (battery or photovoltaic) applications. The interleaved multi-channel converter is very popular these days because of its ability to reduce current ripples. In high power applications, parallel operation of buck converter is recommended. The steady state performance of the interleaved buck converter is investigated by MATLAB/simulation. The IBC is designed for low input voltage application. The modeling and analysis is carried out considering the parasitic elements of all the elements and devices. The IBC is modeled and analyzed using state-space averaging technique and analysis is carried using small signal analysis. The analog PID controller is designed based on the design parameters of the converter and simulated in open loop and closed loop.**

***Index Terms*****—Interleaved Buck converter, small signal analysis, state space technique, continuous conduction mode**

## I. INTRODUCTION

The demand for DC-DC converter has increased as the front end stage for the battery sources and the renewable energy applications. Two Phase Interleaved DC-DC Buck converter is introduced to meet the increased demands such as low current ripple, high efficiency, faster dynamics, light weight and higher power density. Interleaving also called multi-phasing, is a technique that is useful for reducing the size of filter components [5]. IBC performs remarkably in terms of magnetics, input and output current ripple and part count [4]. The Voltage Regulator Modules (VRMs) are used to power the µp (microprocessors) in the computers, make use of the conventional or synchronous buck converters. The VRMs require output voltage lower than 1 volt and output current higher than 100 amperes. This makes the existing topology inadequate. The interleaved dc-dc converters are suitable for the low voltage and high current output topology.. IBC will act as a pre-regulator in the PV system. Interleaved buck converter is used to convert the unregulated DC input voltage into a controlled DC output at a desired voltage level [2].

The Two Phase Interleaved Buck converter was modeled considering all the parasitic elements of the converter using state space average technique [1,2] and analyzed using small signal analysis. The model is simulated in MATLAB/Simulation in open loop and closed loop with analog PID controller.

This paper presents the design of IBC and also modeling and analysis of IBC. Section II presents working principle of IBC. Section III describes the steady state characteristics of buck converter and also design of IBC. Section IV presents modeling and analysis of two phase IBC. Section V gives the simulation results. Finally section VI concludes the paper.

## II. TWO PHASE INTERLEAVED BUCK CONVERTER

The two phase interleaved buck converter is as shown in "Fig.1,". the two converters are essentially connected in parallel but operate in an interleaved mode. The first converter is composed of inductor $L_1$, Switch $S_1$, and Diode $D_1$, where as the second converter consists of $L_2$, $S_2$, and $D_2$. The IBC share the same filter capacitor C at the output. It is assumed that the parameters of the two converter are identical. The gating arrangements and the inductor current waveforms of the convert is shown in "Fig.2,". this figure represents waveforms of inductor current and input current and the converter is operated with duty ratio *d* $(0<d\leq 0.5)$ in this duty ratio any one switch will be conducting at time and also at specific period of time both the inductors will be discharging. With two phase IBC designs, the gating signals $g_1$ and $g_2$ for switch $S_1$ and $S_2$ are identical but shifted by 180˚. The total input current $I_{in}$, which is the sum of the two inductor currents $i_{L1}$ and $i_{L2}$ are shown in "Fig.2".

### *Abbreviations and Acronyms*

$V_{in}$ – Input Voltage, $V_{dc}$ – output Voltage, $I_L$ – Inductor Current, $I_{in}$ – Input Current, $i_{L1}$ , $i_{L2}$ – Current

 

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flowing in inductors $L_1$ and $L_2$, $I_o$ – output Current,
$S_1$, $S_2$ – MOSFETs/Switches
$g_1$, $g_2$ –Gating signals, $D_1$, $D_2$ – Diodes, C – Capacitor d/D – Duty ratio, $\Delta I_{L1}$, $\Delta I_{L2}$ – $L_1$ and $L_2$ Inductor ripple current
$f_{SW}$ – Switching frequency, $P_{in}$ – input power
$i_{D,on}$, $i_{D,off}$ – Diode Current during ON/OFF
$i_{M,on}$, $i_{M,off}$ – MOSFET (switch) current during ON/OFF
$r_{L1}$, $r_{L2}$ – Resistance of Inductors $L_1$ and $L_2$
$r_{S1}$, $r_{S2}$ – On state resistance of switches $S_1$ and $S_2$
R – Load Resistance
$V_{d1}$, $V_{d2}$ – Voltage across $D_1$ and $D_2$
$r_C$ – Resistance of capacitance C

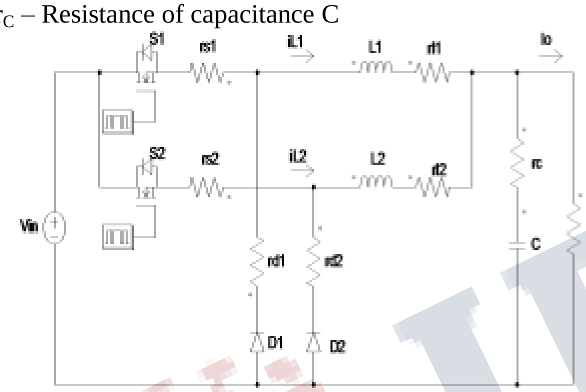


*Fig 1. Two Phase Interleaved Buck Converter*

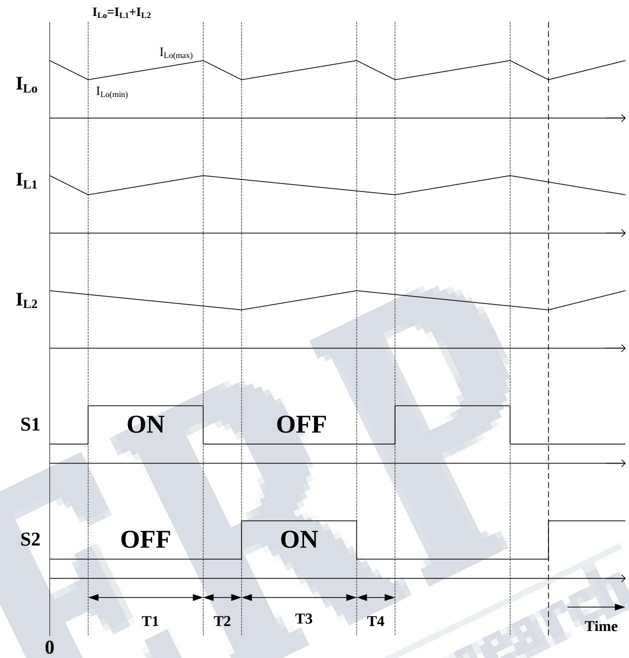


*Fig 2 Typical Waveforms of Inductor Currents*

STEADY STATE CHARACTERISTICS AND DESIGN OF IBC

BUCK RATIO: ***THE BUCK RATIO OF THE CONVERTER IS A FUNCTION OF THE DUTY RATIO.*** $\frac{V_{dc}}{V_{in}} = D$

INPUT CURRENT: ***THE INPUT CURRENT CAN BE CALCULATED BY THE INPUT POWER AND THE INPUT VOLTAGE.*** $I_{in} = \frac{P_{in}}{V_{in}}$

INDUCTOR CURRENT RIPPLE AMPLITUDE:

$$\Delta I_{L1,L2} = \frac{(V_S - V_O)D}{f_{SW} L}$$

***Design of IBC:*** Input data for designing the two phase interleaved buck converter output of 5V from a input of 24V source inductor current is continuous and output ripple of less

 

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than 10%. The output power of 25Watts, switching frequency 25 kHz

Duty ratio (D)

$$D = \frac{V_o}{V_s} = \frac{5}{24} = 0.208$$

$$R = \frac{V_o^{\,2}}{P_o} = \frac{(5)^2}{25} = 1\Omega$$

Inductor (L)

$$L_{\min} = \frac{(1-D)R}{2\times f_{sw}} = 16\mu\text{H}$$

$$L = 1.25\times L_{\min} = 20\mu\text{H}$$

$$L_1 = L_2 = \frac{L}{2} = 10\mu\text{H}$$

Load Current

$$I_L = \frac{V_o}{R} = 5A$$

$$I_{L1} = I_{L2} = \frac{I_L}{2} = 2.5A$$

Ripple Inductor Current

$$\Delta i_L = \frac{(V_s - V_o)D}{L\times f} = 7.904A$$

Capacitor (C)

$$C = \frac{(1-D)}{8L\left(\frac{\Delta V_o}{V_o}\right)f^2} = 80\mu F$$

Maximum and Minimum Inductor Current

$$i_{L\max} = I_L + \frac{\Delta i_L}{2} = 8.952A$$

$$i_{L\min} = I_L - \frac{\Delta i_L}{2} = 1.048A$$

Equivalent series resistance (ESR)

$$\Delta V_{o(ESR)} = \Delta i_c r_c$$

$$\Delta i_c = i_{L\max}$$

$$r_c = \frac{\Delta V_{o(ESR)}}{\Delta i_c} = 0.066\Omega$$

$$Efficiency\ \eta = \frac{P_O}{P_O + P_{LOSS}} = 97.59\%$$

## III. MODELLING AND ANALYSIS OF TWO PHASE BUCK CONVERTER

### *A. Modeling*

Analysis of two phase interleaved buck converter using state space averaging technique. The two phase interleaved buck converter is analyzed for duty cycle (0<d≤0.5). The circuit can be analyzed in four modes of operation by considering parasitic elements.

**MODE – 1** Switch $S_1$ is closed and $S_2$ is open, in this period inductor current $i_{L1}$ is rising and $i_{L2}$ is falling as shown in "Fig.2,"

Analyze the "Fig.3," by applying KVL and KCl we get the equation in matrix form

State variables are $\begin{bmatrix} i_{L1} \\ i_{L2} \\ V_C \end{bmatrix}$

$$A1 = \begin{bmatrix} \frac{1}{L_1}\left[(-r_{L1}-r_{S1}) - \frac{R_{Load}r_C}{(R_{Load}+r_C)}\right] & 0 & -\frac{1}{L_1}\left(\frac{R_{Load}}{(R_{Load}+r_C)}\right) \\ 0 & \frac{1}{L_2}\left[(-r_{L2}-r_{D2}) + \frac{R_{Load}r_C}{(R_{Load}+r_C)}\right] & \frac{1}{L_2}\left(\frac{R_{Load}}{(R_{Load}+r_C)}\right) \\ \frac{R_{Load}}{2C(R_{Load}+r_C)} & \frac{R_{Load}}{2C(R_{Load}+r_C)} & \frac{-1}{C(R_{Load}+r_C)} \end{bmatrix}$$

$$B1 = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 \\ 0 & 0 & \frac{-1}{L_2} \\ 0 & 0 & 0 \end{bmatrix}$$

$$C1 = \begin{bmatrix} \frac{R_{Load}r_C}{(R_{Load}+r_C)} & \frac{R_{Load}r_C}{(R_{Load}+r_C)} & \frac{R_{Load}}{(R_{Load}+r_C)} \end{bmatrix}$$

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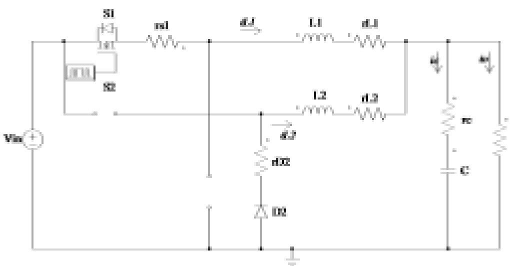


*Fig 3 Mode 1 Operation*

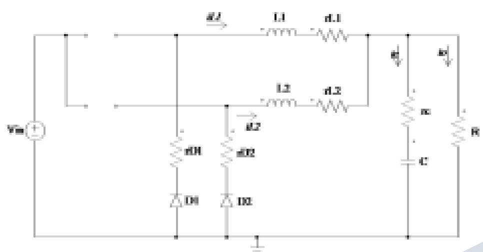


*Fig 4 Mode 2 Operation*

**Mode – 2** Switch $S_1$ and $S_2$ is open, in this period both the inductor current $i_{L1}$ and $i_{L2}$ is falling as shown in "Fig.2,"

$$A2=\begin{bmatrix} \frac{1}{L_1}\left[(-r_{L1}-r_{D1})+\frac{R_{Load}r_C}{(R_{Load}+r_C)}\right] & 0 & \frac{1}{L_1}\left(\frac{R_{Load}}{(R_{Load}+r_C)}\right) \\ 0 & \frac{1}{L_2}\left[(-r_{L2}-r_{D2})+\frac{R_{Load}r_C}{(R_{Load}+r_C)}\right] & \frac{1}{L_2}\left(\frac{R_{Load}}{(R_{Load}+r_C)}\right) \\ \frac{R_{Load}}{2C(R_{Load}+r_C)} & \frac{R_{Load}}{2C(R_{Load}+r_C)} & \frac{-1}{C(R_{Load}+r_C)} \end{bmatrix}$$

$$B2=\begin{bmatrix} 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & \frac{-1}{L_2} \\ 0 & 0 & 0 \end{bmatrix}$$

$$C2=\begin{bmatrix} \frac{R_{Load}r_C}{(R_{Load}+r_C)} & \frac{R_{Load}r_C}{(R_{Load}+r_C)} & \frac{R_{Load}}{(R_{Load}+r_C)} \end{bmatrix}$$

**Mode – 3** Switch $S_1$ is open and $S_2$ is closed, in this period inductor current $i_{L1}$ is falling and $i_{L2}$ is rising as shown in "Fig.2,"

$$A3=\begin{bmatrix} \frac{1}{L_1}\left[(-r_{L1}-r_{D1})+\frac{R_{Load}r_C}{(R_{Load}+r_C)}\right] & 0 & \frac{1}{L_1}\left(\frac{R_{Load}}{(R_{Load}+r_C)}\right) \\ 0 & \frac{1}{L_2}\left[(-r_{L2}-r_{D2})-\frac{R_{Load}r_C}{(R_{Load}+r_C)}\right] & \frac{-1}{L_2}\left(\frac{R_{Load}}{(R_{Load}+r_C)}\right) \\ \frac{R_{Load}}{2C(R_{Load}+r_C)} & \frac{R_{Load}}{2C(R_{Load}+r_C)} & \frac{-1}{C(R_{Load}+r_C)} \end{bmatrix}$$

$$B3=\begin{bmatrix} 0 & \frac{-1}{L_1} & 0 \\ \frac{1}{L_2} & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

$$C3=\begin{bmatrix} \frac{R_{Load}r_C}{(R_{Load}+r_C)} & \frac{R_{Load}r_C}{(R_{Load}+r_C)} & \frac{R_{Load}}{(R_{Load}+r_C)} \end{bmatrix}$$

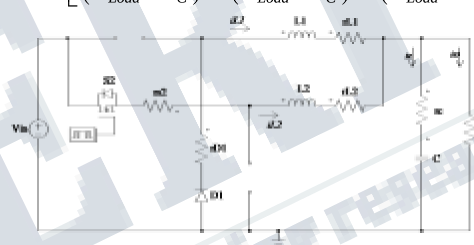


*Fig 5 Mode 3 Operation*

***Mode – 4*** Switch $S_1$ and $S_2$ is open, in this period both the inductor current $i_{L1}$ and $i_{L2}$ is falling as shown in "Fig.2,"

$$A4=\begin{bmatrix} \frac{1}{L_1}\left[(-r_{L1}-r_{D1})+\frac{R_{Load}r_C}{(R_{Load}+r_C)}\right] & 0 & \frac{1}{L_1}\left(\frac{R_{Load}}{(R_{Load}+r_C)}\right) \\ 0 & \frac{1}{L_2}\left[(-r_{L2}-r_{D2})+\frac{R_{Load}r_C}{(R_{Load}+r_C)}\right] & \frac{1}{L_2}\left(\frac{R_{Load}}{(R_{Load}+r_C)}\right) \\ \frac{R_{Load}}{2C(R_{Load}+r_C)} & \frac{R_{Load}}{2C(R_{Load}+r_C)} & \frac{-1}{C(R_{Load}+r_C)} \end{bmatrix}$$

$$B4=\begin{bmatrix} 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & \frac{-1}{L_2} \\ 0 & 0 & 0 \end{bmatrix}$$

$$C4=\begin{bmatrix} \frac{R_{Load}r_C}{(R_{Load}+r_C)} & \frac{R_{Load}r_C}{(R_{Load}+r_C)} & \frac{R_{Load}}{(R_{Load}+r_C)} \end{bmatrix}$$

***Analysis***

Based on the assumption that all switching cells carry equal average current and are operating at the same duty ratio in a switching cycle of interest,
We obtain

$$d_{2i-1} = d \;\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$d_{2i} = \frac{1}{N} - d \;\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

$$i = 1, 2 \ldots\ldots\ldots\ldots N$$

$d$ - Duty ratio

If $d$ is constant from cycle to cycle, it is defined as the steady-state duty ratio, D.
Average state space model over one particular cycle can be written as

$$\dot{\boldsymbol{x}} = \boldsymbol{Ax} + \boldsymbol{BV_s} \;\ldots\ldots\ldots\ldots\ldots\ldots \mathbf{(3)}$$

By applying (2) to the waveforms in figure , we obtain

$$A = \sum_{j=1}^{2N} d_j A_j \;\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

$$B = \sum_{j=1}^{2N} d_j B_j \;\ldots\ldots\ldots\ldots\ldots\ldots (5)$$

$$C = \sum_{j=1}^{2N} d_j C_j \;\ldots\ldots\ldots\ldots\ldots\ldots (6)$$

Where $A_j$ and $B_j$ are the state matrix and the control vector of the interval $d_jT_S$ respectively, and $j$=1,2. . . . . . . . 2N.
We now assume that $d$ = $D$. Using equations (1) and (2) in equation (4), we can write

$$A = D\sum_{i=1}^{N} A_{2i-1} + \left(\frac{1}{N} - D\right)\sum_{i=1}^{N} A_{2i} \;\ldots\ldots\ldots (7)$$

similarly we can write (5)

$$B = D\sum_{i=1}^{N} B_{2i-1} + \left(\frac{1}{N} - D\right)\sum_{i=1}^{N} B_{2i} \;\ldots\ldots\ldots (8)$$

similarly we can write (6)

$$C = D\sum_{i=1}^{N} C_{2i-1} + \left(\frac{1}{N} - D\right)\sum_{i=1}^{N} C_{2i} \;\ldots\ldots\ldots (9)$$

Substituting N=2 in the above equations we get

$$A = (A_1 + A_3)(1-D) + (2D-1)A_2$$
$$B = (B_1 + B_3)(1-D) + (2D-1)B_2 \qquad \ldots\ldots\ldots\ldots (10)$$
$$C = (C_1 + C_3)(1-D) + (2D-1)C_2$$

To investigate the small-signal behavior, we now assume that d varies from cycle to cycle. Equation (7) (8) and (9) are the perturbations in the input voltage, in the duty ratio and in the states are introduced to (3).

By neglecting the non-linear second-order term, the perturbed state-space equation for an N-phase interleaved converter is obtained as

$$\dot{\tilde{x}} = AX + BV + A\tilde{x} + B\tilde{V}_S + \left[\sum_{i=1}^{N}(A_{2i-1} - A_{2i})X + \sum_{i=1}^{N}(B_{2i-1} - B_{2i})V_S\right]\tilde{d}$$

When al, perturbations are set to zero, the steady-state model is obtained as

$$\boldsymbol{X = -A^{-1}BV_S}$$

Consequently, the small signal model is found to be as

$$\dot{\tilde{x}} = A\tilde{x} + B\tilde{V}_S + \left[\sum_{i=1}^{N}(A_{2i-1} - A_{2i})X + \sum_{i=1}^{N}(B_{2i-1} - B_{2i})V_S\right]\tilde{d}$$

$$\dot{\tilde{x}} = A\tilde{x} + B\tilde{V}_S + \left[(A_1 + A_3 - 2A_2)X + (B_1 + B_3 - 2B_2)V_S\right]\tilde{d}$$

Applying laplace transform

$$s\tilde{x}(s) = A\tilde{x}(s) + B\tilde{V}_S(s) +$$
$$\left[(A_1 + A_3 - 2A_2)X + (B_1 + B_3 - 2B_2)V_S\right]\tilde{d}(s)$$

$$\tilde{x}(s) = [sI - A]^{-1}$$
$$\left[B\tilde{V}_S(s) + \left[(A_1 + A_3 - 2A_2)X + (B_1 + B_3 - 2B_2)V_S\right]\right]\tilde{d}(s)$$

let us now assume

$$K = \left[(A_1 + A_3 - 2A_2)\right]$$

$$T = \left[(B_1 + B_3 - 2B_2)\right]$$

$$\tilde{x}(s) = [sI - A]^{-1}\left[B\tilde{V}_S(s) + \left[(K)X + (T)V_S\right]\right]\tilde{d}(s)$$

$$\tilde{v}_o(s) = C^T\tilde{x}(s)$$

$$\tilde{v}_o(s) = C^T[sI - A]^{-1}\left[B\tilde{V}_S(s) + \left[(K)X + (T)V_S\right]\right]\tilde{d}(s)$$

$$\tilde{v}_o(s) = C^T\tilde{x}(s)$$

$$V_o = \left[(C_1 + C_3)(1-d) + (2d-1)C_2\right]X$$

$$v_o = V_o + \tilde{v}_o \;\;;\;\; x = X + \tilde{x} \;\;;\;\; d = D + \tilde{d}$$

$$v_o = \left(V_o + \tilde{v}_o\right) = \left[(C_1 + C_3)\left(1 - \left(D + \tilde{d}\right)\right) + \left(2\left(D + \tilde{d}\right) - 1\right)C_2\right]\left(X + \tilde{x}\right)$$

$$v_o = \left(V_o + \tilde{v}_o\right) = \left[(C_1 + C_3)\left(1 - D - \tilde{d}\right) + \left(2D + 2\tilde{d} - 1\right)C_2\right]\left(X + \tilde{x}\right)$$

 

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The product of small signals is zero, after simplifying the above equation. We get

$$\hat{v}_o = \left[(C_1 + C_3)(1-D) + (2D-1)C_2\right]\hat{x}$$
$$+\left[(2C_2 - C_1 - C_3)X\right]\hat{d}$$

let us now assume

$$P = \left[(C_1 + C_3)(1-D) + (2D-1)C_2\right]$$
$$Q = (2C_2 - C_1 - C_3)$$
$$\hat{v}_o = [P]\hat{x}(s) + [QX]\hat{d}(s)$$

We know that

$$\hat{x}(s) = [sI - A]^{-1}\left[B\hat{V}_S + \left[(K)X + (T)V_S\right]\right]\hat{d}$$

substituting $\hat{x}(s)$ in the voltage equation

$$\hat{v}_o(s) = P[sI - A]^{-1}\left[B\hat{V}_S(s) + \left[(K)X + (T)V_S\right]\right]\hat{d}(s) + [QX]\hat{d}(s)$$

substituting $B\hat{V}_S(s) = 0$

$$\hat{v}_o(s) = \mathrm{P}[sI - A]^{-1}\left[(K)X + (T)V_S\right]\hat{d}(s) + [QX]\hat{d}(s)$$

Finally, the transfer function of output to variation in the duty ratio is expressed as

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = P[sI - A]^{-1}\left[(K)X + (T)V_s\right] + [QX]$$

Finally by substituting the above equations with their respective values, we obtain the transfer function as follows,

$$G(s) = \frac{s^2(177163.99) + s(1.887954\times10^{10}) + (7.8026\times10^{13})}{s^3 + s^2(23606.07) + s(1181050336) + (6.5807\times10^2)}$$

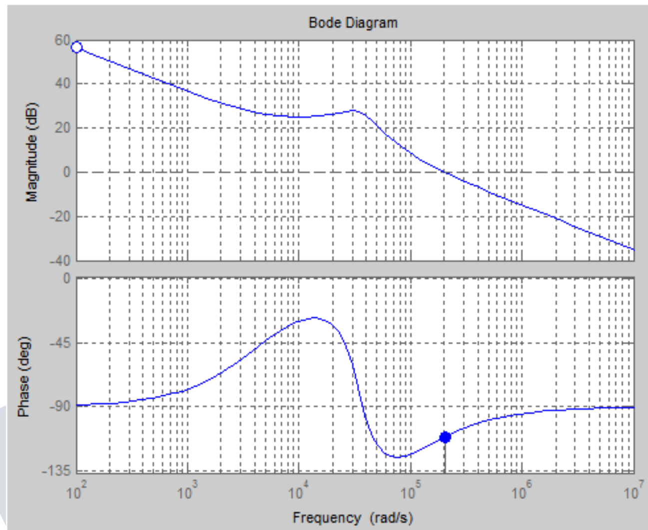


*Fig 6 System Bode Plot*

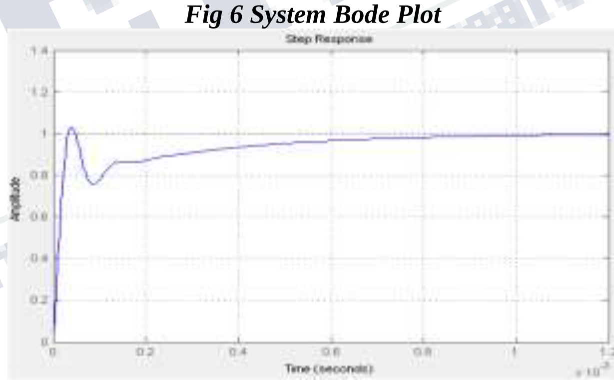


**Fig 7 Closed Loop Step Response**

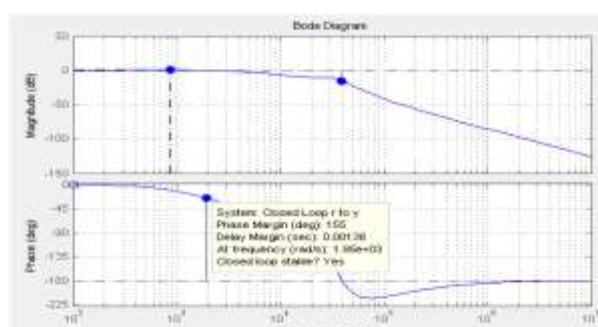


**Fig 8 Closed Loop Bode**

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After obtaining the transfer function of the converter, the same is fed into the SISO design tool command in the MATLAB to generate bode of the system "Fig.6,", closed loop response of compensated system "Fig.7,", closed loop bode "Fig.8," gives the analysis plot. And also using automated PID tuning we can find the $K_p$, $K_i$, and $K_d$ values [$K_p$= 0.06256, $K_i$=641.125 and $K_d$=0]. The same values are fed in to the PID controller these values are set into the PID controller.

## IV. SIMULATION RESULTS

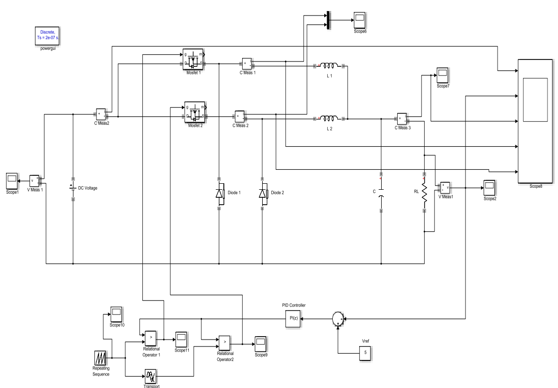

*Fig 9 Two Phase IBC in Closed Loop*

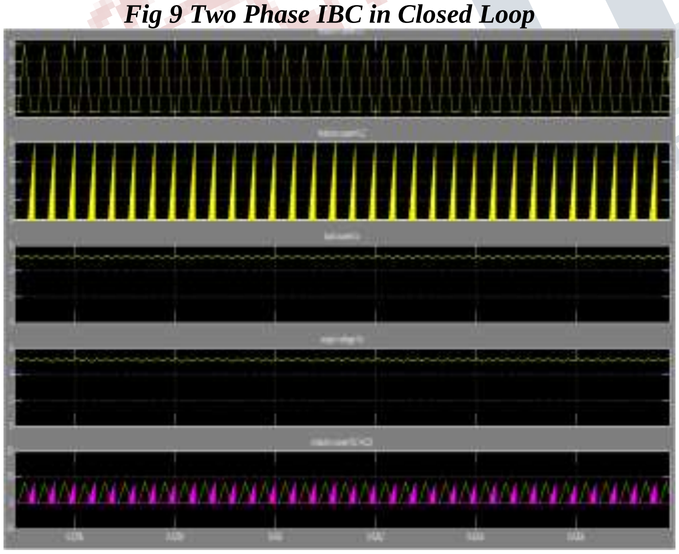

*Fig 10 Voltage and Current Waveforms in Simple PID Controller*

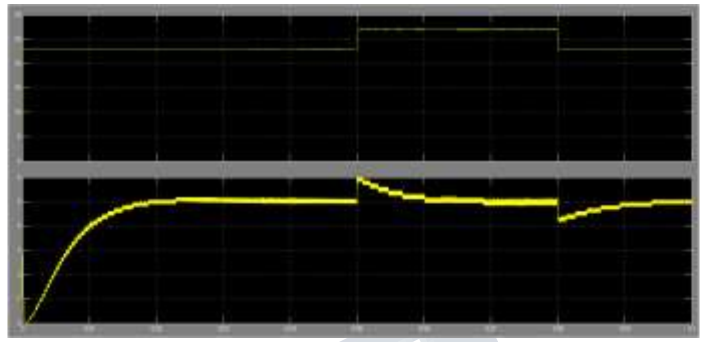

*Fig 11 Output Voltage waveform in Simple PID Controller (+10% Variation in Input Voltage)*

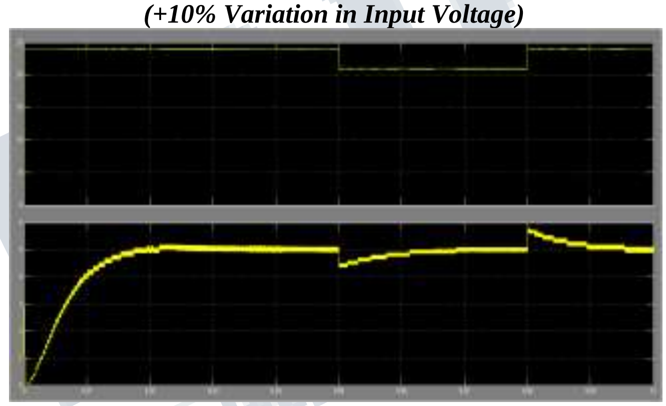

*Fig 12 Output Voltage waveform in Simple PID Controller (-10% Variation in Input Voltage)*

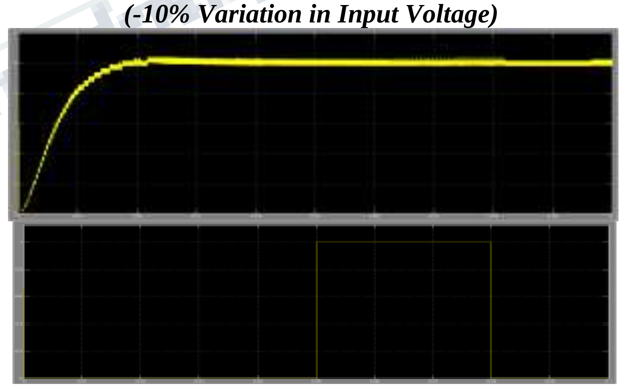

*Fig 13 Output Voltage waveform in Simple PID Controller (+10% Variation in Load)*

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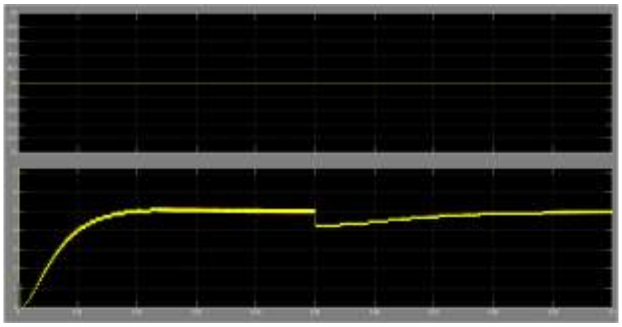

*Fig 14 Output Voltage waveform (Variation in Load keeping the Input Voltage Constant)*

"Fig.9," shows the two phase IBC in closed loop using analog PID controller. "Fig.10," shows results of analog PID controller output voltage and inductor current waveforms. The source current $I_{in}$ is the sum of $I_{L1}$ and $I_{L2}$ as they are in phase opposition, therefore the ripple cancellations in the source current ripple gets reduced. An observed in the current waveforms $I_{in}$ the ripple current $\Delta i_L$ is 7.904A. whereas the ripple current in individual inductor is 2.5A. "Fig.11," and "Fig.12,", shows the simulation results of output voltage waveforms with ±10% variations in input voltage in analog PID controller. The transients at the output voltage waveforms are observed in the rise time and fall time. "Fig.13," and "Fig.14,", shows the simulation results of output voltage waveforms with ±10% load variations and keeping the input voltage constant and varying the load in analog PID controller.

## V. CONCLUSION

The two phase interleaved buck converter is modeled using state space averaging technique considering all parasitic elements of the converter which gives the accurate modeling of the converter. The modeling is analyzed based on small signal analysis to find the transfer function output voltage to variations in duty ratio. This results the perfect modeling of the converter and gives the accurate results. The two phase interleaved buck converter has advantages based on comparison with a single buck converter. The input current and output voltage ripple will be reduced and also the size of filtering component at the output. By increasing the number of levels of the converter, will result in the reduction of the size of the filter and source current ripple and increase the power density and efficiency of the converter.

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