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Design of Low Drop Out voltage regulator for low power applications

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Abstract-— **As the technology is being scaled down leakage power is becoming an important contributing factor in total power dissipation in the circuit. So in the portable devices such as cell phones, laptops emphasis has to be given to reduce power consumption during active as well as standby mode. This paper presents the Design of LDO voltage regulator. This work aims at further reduction in power consumption and drop out voltage using Floating gate pass transistor. A comparison of different Low Drop out regulator using various pass transistor logic is proposed and the Designed LDO shows a reduction of drop out voltage of 15.38% in the circuit. This circuit is simulated in 180nm CMOS Technology.**

I. INTRODUCTION:

In current scenario , with the feature size being reduced in As the scale of integration improves, more transistors, faster and smaller than their predecessors, are being packed into a chip. This leads to the steady growth of the operating frequency and processing capacity per chip, resulting in increased power dissipation. Another factor that fuels the needs for low power chips is the increased market demand for portable consumer electronics powered by batteries. The regulator is an essential part in battery powered mobile devices. In a system, with continuous discharge of battery voltage over time, these regulators can provide a constant voltage to the circuits. LDO provides relatively high efficiency due to the small difference between its input and output voltages. The LDO is used in power management system. Power management helps to improve the device power efficiency resulting in increasing the battery life that helps to operate the device for a longer period time. A power management system contains several blocks including linear voltage regulators, switching regulator and control logic system. The control logic changes the attributes of each block i.e. controlling the outputs data either to a low or high as well as changing the output voltage levels, to optimize the power consumption of the device.

The voltage regulator presented in this paper is designed for low power analog circuits, where the power consumption is in the range of few µWatts. A general block diagram of such low power sensing device contains several blocks as well as Low drop out regulators as shown in Fig.1. A power-efficient linear voltage regulator, that converts variable voltages generated from switching converter into a constant output voltage.

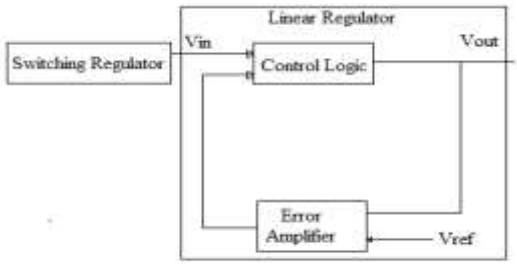

Fig.1. The general block diagram of LDO voltage regulator.

For mobile electronic devices such as cell phones and PDAs, low power consumption is a very significant requirement to extend the battery life for a longer period. Thus, the low voltage and low quiescent current are the most important parameters to achieve high power efficiency for battery devices. However, the LDO regulators suffer from the trade-off problem between power consumption with other important design parameters such as drop out voltage and transient response. This can be eliminated by using Floating gate nMOS transistor and by using the resistive feedback element.

The drop out voltage is defined as the difference between input and output voltage such that it converts fluctuating input value to a constant output voltage. The basic LDO block contains pass transistor, error amplifier and resistive feedback elements.

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II. LDO TOPOLOGIES

A. LDO Using pMOS Pass Transistor

Traditionally, a pMOS pass transistor is adopted in an LDO, as shown in Fig. 2. to achieve a low drop-out voltage. Assuming that a type-B error amplifier is used, the supply noise is amplified through the pMOS pass transistor and the line regulation can be expressed as

$$\text{Line Regulation (pMOS)} = \frac{V_{out}}{V_{in}} X\ 100$$

If the load current varies, the LDO output voltage is regulated through the error sensing amplifier by adjusting the gate voltage of the pMOS pass transistor. For fast transient response, it is necessary to design an error amplifier with large bandwidth at the cost of power consumption.

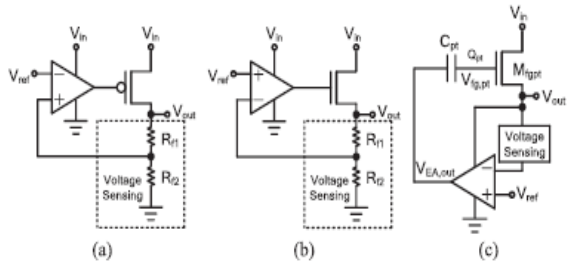

Fig.2. (a) A conventional voltage regulator uses a pMOS pass transistor for a low drop-out voltage. (b) An alternative conventional voltage regulator topology uses a nMOS pass transistor for line regulation improvement but with the drop-out voltage of VGS. (c)The proposed LDO voltage regulator that uses Floating gate transistor.

B. LDO Using nMOS Pass Transistor

The nMOS transistor is used as pass transistor which is connected in series with load as shown in below Fig. 3.
The LDO voltage regulator is implemented by using nMOS pass transistor that is connected between the input and the load as shown in Fig. 3.
The main advantage of using nMOS transistor compared to pMOS transistor is that it has a line regulation i.e. there is less drop at load around 300mV. Another advantage of using nMOS is that the transient response is good compared to pMOS transistor as mobility of the nMOS transistor is two times that of pMOS transistor.

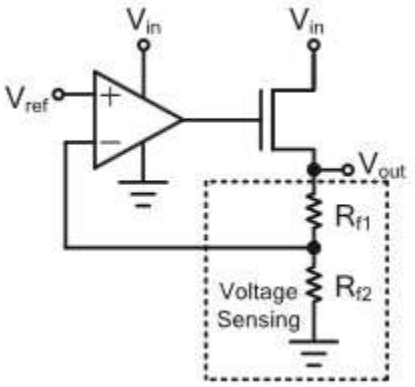

Fig. 3. The block diagram of LDO with nMOS pass transistor.

The input voltage Vin is given to the drain terminal of the pass transistor Vin=1.8v and the output is taken from the source terminal across the resistor. A part of output is fed back to the error amplifier which is sensed by the resistors. The output of the error amplifier which is an error voltage is sent to the pass transistor in order to improve the slew rate.

$$\text{Line Regulation (nMOS)} = \frac{V_{out}}{V_{in}} X\ 100$$

For nMOS pass device, there is a trade-off between line regulation and power consumption is present. The line regulation can be improved with a loss of more power consumption as compared to pMOS pass transistor. These trade-off can be overcome by using Floating gate pass transistor.

C. Proposed LDO using nMOS capacitor or floating gate pass transistor

In this work, a floating gate pass transistor is used to overcome the drawback of nMOS i.e. line regulation and power consumption at the load.
The floating gate contains basically nMOS and a capacitor used to improve the transient response of the device. With the help of F-N tunnelling method the charge which is stored in the capacitor of floating gate will restrain for a longer period of time. With the help of this charge, the pass device can turned on within a short

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period of time. Due to which transient response can be improved as well as the output voltage can be preserved at load for a longer period of time in order to work the device for a longer time.
The maximum output voltage can be achieved by sizing the transistor width, resistor values and with the help of floating gate transistor.
The resistor values can be obtained by

$$R1 + R2 = \frac{V_{out}}{I_L}$$

The proposed LDO Block diagram mainly contains three sub-blocks i.e. Error amplifier, Floating gate as a pass transistor, feedback sensing elements, and reference voltage.

III. PROPOSED LDO CIRCUIT IMPLEMENTATION

A. Adaptively Biased Class-AB Error Amplifier

The error amplifier in an LDO is crucial for both line and load regulation. Multistage topologies are usually adopted with carefully designed compensation schemes to ensure circuit stability. To reduce circuit complexity for compensation and to achieve high line regulation as well as load regulation, in the proposed LDO, a regulated folded cascode scheme is adopted in the error amplifier design for high open-loop gain. As shown in Fig. 3.1, the proposed error amplifier employs a class-AB input differential pair and is adaptively biased to improve its transient responses under the stringent constraint of extremely low quiescent current consumption.

The bandwidth of the amplifier can be tuned by programming the charge, Q_{bias} on a bias floating- gate transistor, M_8. The employed class-AB differential pair, which was firstly proposed, is based on a bump circuit consisting of transistors M_1-M_7. To keep the I-V characteristics of the bump circuit symmetrical, transistors, M_3-M_6, are employed in Fig. 3.2. With this symmetrical topology to replace the series transistors. If all transistors are biased in the sub-threshold region, the bump current, I_{bump}, is proportional to the harmonic mean of I_1 and I_2 as long as transistors M_4 and M_6 are biased in the saturation region, although transistors M_3 and M_5 can be in the ohmic region. By keeping $I_{bump-constant}$ using the feedback connection from the drain terminals of M_4 and M_6 to the gate terminal of the tail transistor, M_7, the current difference, I_1-I_2, exhibits class-AB push- pull characteristics with detailed analytical expressions derived.

Although the input common-mode range of the class-AB input stage is limited by keeping M4, M6, M7 in saturation, the proposed floating gate approach allows the input voltage being programmed in the proper region with the maximum input swing range as will be explained in the next subsection. When the LDO is at quiescence, two input voltages V_{ref} and V_{sense} are equal. The bump current, I_{bump}, which is set by I_{bias}, dominates I_{tail}. In this state, all current levels can be relatively small. When LDO load current changes abruptly, the difference between V_{ref} and V_{sense} increases, resulting in I_{bump} reduction. Since the I_{bias}, which is set by Q_{bias}, remains constant, the voltage, V_{bn}, will be charged up until I_{bump} = I_{bias}, leading to dramatic increase in I_{tail}. The increment of I_{tail} will be steered to the output stage through either I_1 or I_2, depending on the input polarity. Consequently, during the transient period, the output voltage would be pushed or be pulled by currents much larger than the quiescent current

To enhance LDO line regulation, the error amplifier output branches adopt regulated cascode topologies for gain boosting. Since Itail is small at quiescence and increases dramatically at transient, the bias current levels at the output branches are also adaptively biased by Vbn. The amplifiers used for gain boosting are composed of a common-source amplifier following a source follower, which shifts the sensing voltage level, Vsp or Vsn, by one |VGS|. As a result, the |VDS| of transistorsM15, M16 or M9, M10 can be one VDSsat instead of one |VGS| to increase the output swing range. To avoid the output overshoot voltage stressing circuits connected to the LDO, during the start-up phase, the input stages of the common-source amplifiers are pMOS transistors. During the early start-up phase, the regulating common-source amplifier output voltage, Vcasp or Vcasn, follows the

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amplifier supply voltage, VLDO,out, so that the cascade pMOS transistors, M11,M12, are off and the cascode nMOS transistors, M13,M14 are on.

The error amplifier output is thus close to ground to prevent the pass transistor from turning on fully. Once the LDO output voltage increases to a level such that the regulating common source amplifiers are fully operational, the cascode voltages will be regulated normally to enhance the error amplifier open loop gain.

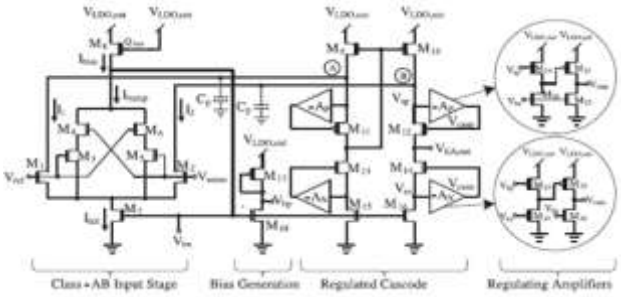


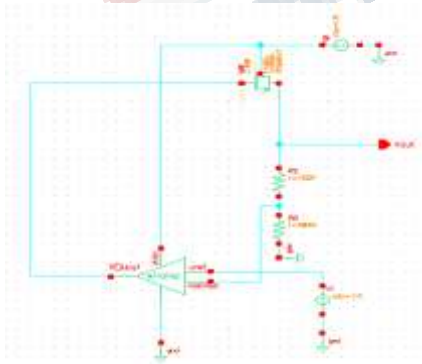
Fig. 4. The internal structure of Error amplifier with gain amplifier AN and AP.

B. Resistive feedback sensing elements

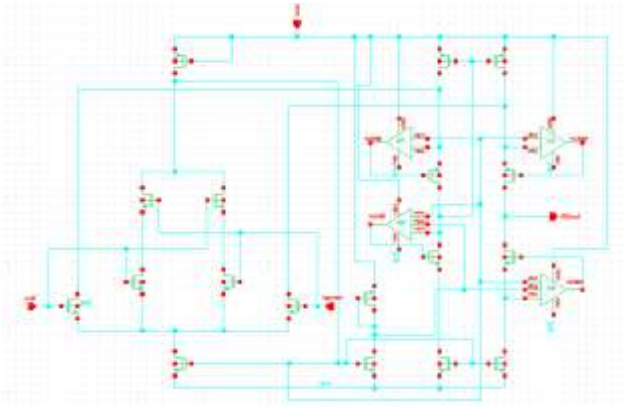
The resistive feedback element is used to sense the output voltage change with respective to the change in input voltage.

IV. SIMULATION RESULTS

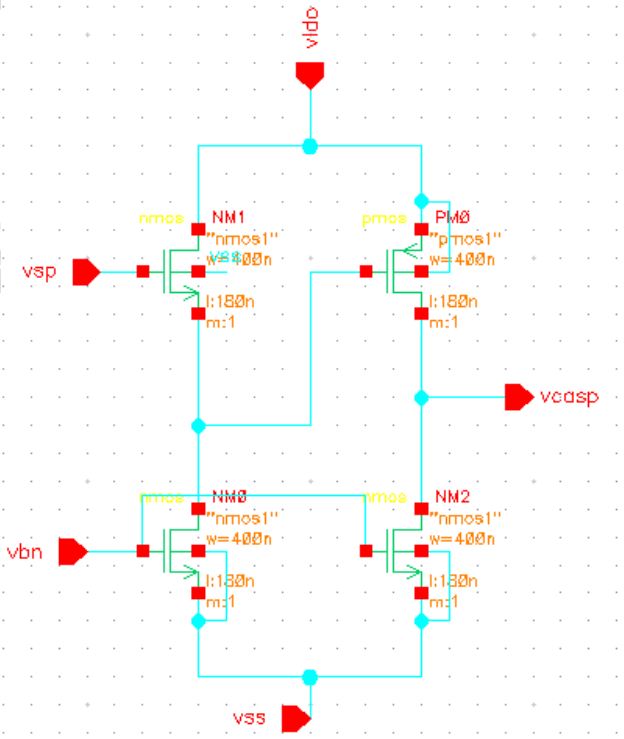
A. Proposed Design of LDO using Floating gate nMOS transistor



B. Internal structure of the error amplifier with W= 2µm



C. Gain amplifier AP with W= 400nm



D. Gain amplifier AN with W= 500nm

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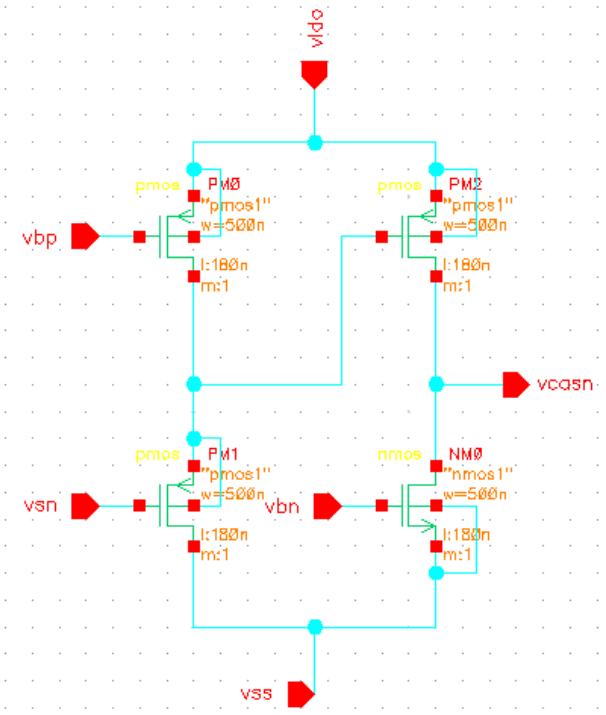
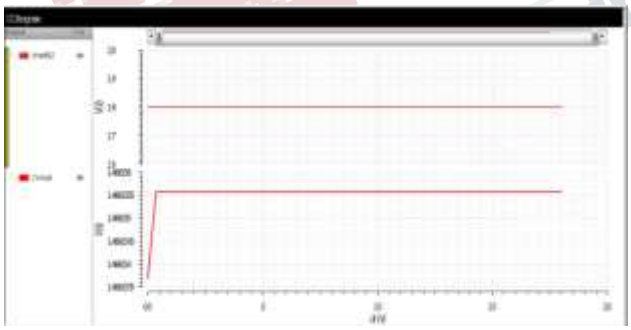


E. Output of LDO using Floating gate nMOS transistor for Vin= 1.8V



F. Comparison of LDO voltage regulator with nMOS, pMOS and floating gate nMOS transistor.

Vin=1.8v	pMOS	nMOS	Floating gate nMOS
Output Voltage	1.1v	1.3v	1.5v
Power consumption	603.5µw	617.8µw	564.2µw
Transient response	Good	Better	Best

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