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Voltage and Power Flow Control of Dual Voltage Source Inverter

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***Abstract*: -- This paper presents a dual voltage source inverter (DVSI) scheme to enhance the power quality and reliability of the microgrid system. The proposed scheme is comprised of two inverters, which enables the microgrid to exchange power generated by the distributed energy resources (DERs) and also to compensate the local unbalanced and nonlinear load. The control algorithms are developed based on instantaneous symmetrical component theory (ISCT) to operate DVSI in grid sharing and grid injecting modes. The proposed scheme has increased relia-bility, lower bandwidth requirement of the main inverter, lower cost due to reduction in filter size, and better utilization of micro-grid power while using reduced dc-link voltage rating for the main inverter. These features make the DVSI scheme a promising option for microgrid supplying sensitive loads. The topology and control algorithm are validated through extensive simulation and experimental results.**

Index Terms—Grid-connected inverter, instantaneous symmet-rical component theory (ISCT), microgrid, power quality..

I. INTRODUCTION

Technological progress and environmental concerns drive the power system to a paradigm shift with more renewable energy sources integrated to the network by means of distributed generation (DG). These DG units with coordinated control of local generation and storage facilities form a microgrid [1]. In a microgrid, power from different renewable energy sources such as fuel cells, photovoltaic (PV) systems, and wind energy systems are interfaced to grid and loads using power electronic converters. A grid interactive inverter plays an important role in exchanging power from the microgrid to the grid and the connected load [2],[3]. This microgrid inverter can either work in a grid sharing mode while supplying a part of local load or in grid injecting mode, by injecting power to the main grid.

Maintaining power quality is another important aspect which has to be addressed while the microgrid system is connected to the main grid. The proliferation of power electronics devices and electrical loads with unbalanced nonlinear currents has degraded the power quality in the power distribution net-work. Moreover, if there is a considerable amount of feeder Manuscript received April 24, 2014; revised November 09, 2014; accepted December 04, 2014. This work was supported by the Department of Science and Technology, India under the Project Grant DST/TM/SERI/2k10/47(G). Paper no. TSTE-00176-2014.

The authors are with the Department of Electrical Engineering, Indian Institute of Technology Madras, Chennai 600036, India (e-mail: yemvee1975@ gmail.com; mahesh@ee.iitm.ac.in; chandan3107@gmail.com). Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org. Digital Object Identifier 10.1109/TSTE.2014.2386534 impedance in the distribution systems, the propagation of these harmonic currents distorts the voltage at the point of common coupling (PCC). At the same instant, industry automation has reached to a very high level of sophistication, where plants like automobile manufacturing units, chemical factories, and semiconductor industries require clean power. For these appli-cations, it is essential to compensate nonlinear and unbalanced load currents [4]. Load compensation and power injection using grid interac-tive inverters in microgrid have been presented in the literature [5],
[6]. A single inverter system with power quality enhance-ment is discussed in [7]. The main focus of this work is to realize dual functionalities in an inverter that would provide the active power injection from a solar PV system and also works as an active power filter, compensating unbalances and the reactive power required by other loads connected to the system.

In [8], a voltage regulation and power flow control scheme for a wind energy system (WES) is proposed. A distribu-tion static compensator (DSTATCOM) is utilized for voltage regulation and also for active power injection. The control scheme maintains the power balance at the grid terminal during the wind variations using sliding mode control. A multifunc-tional power electronic converter for the DG power system is described in [9]. This scheme has the capability to inject power generated by WES and also to

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perform as a harmonic compen-sator. Most of the reported literature in this area discuss the topologies and control algorithms to provide load compensa-tion capability in the same inverter in addition to their active power injection. When a grid-connected inverter is used for active power injection as well as for load compensation, the inverter capacity that can be utilized for achieving the second objective is decided by the available instantaneous microgrid real power [10]. Considering the case of a grid-connected PV inverter, the available capacity of the inverter to supply the reac-tive power becomes less during the maximum solar insolation periods [11]. At the same instant, the reactive power to regu-late the PCC voltage is very much needed during this period [12]. It indicates that providing multifunctionalities in a sin-gle inverter degrades either the real power injection or the load compensation capabilities.

This paper demonstrates a dual voltage source inverter (DVSI) scheme, in which the power generated by the microgrid is injected as real power by the main voltage source inverter (MVSI) and the reactive, harmonic, and unbalanced load compensation is performed by auxiliary voltage source inverter (AVSI). This has an advantage that the rated capacity of MVSI can always be used to inject real power to the grid, if sufficient renewable power is available at the dc link. In the DVSI scheme, as total load power is supplied by two inverters, power losses across the semiconductor switches of each inverter are reduced. This increases its reliability as compared to a single inverter with multifunctional capabilities [13]. Also, smaller size modular inverters can operate at high switching frequen-cies with a reduced size of interfacing inductor, the filter cost gets reduced [14]. Moreover, as the main inverter is supplying real power, the inverter has to track the fundamental positive sequence of current. This reduces the bandwidth requirement of the main inverter. The inverters in the proposed scheme use two separate dc links. Since the auxiliary inverter is supplying zero sequence of load current, a three-phase three-leg inverter topology with a single dc storage capacitor can be used for the main inverter. This in turn reduces the dc-link voltage requirement of the main inverter. Thus, the use of two separate inverters in the proposed DVSI scheme provides increased reliability, better utilization of microgrid power, reduced dc grid voltage rating, less bandwidth requirement of the main inverter, and reduced filter size [13]. Control algorithms are developed by instantaneous symmetrical component theory (ISCT) to operate DVSI in grid-connected mode, while con-sidering nonstiff grid voltage [15], [16]. The extraction of fundamental positive sequence of PCC voltage is done by dq0 transformation [17]. The control strategy is tested with two parallel inverters connected to a three-phase four-wire distribu-tion system. Effectiveness of the proposed control algorithm is validated through detailed simulation and experimental results.

II. DUAL VOLTAGE SOURCE INVERTER

A. System Topology

The proposed DVSI topology is shown in Fig. 1. It con-sists of a neutral point clamped (NPC) inverter to realize AVSI and a three-leg inverter for MVSI [18]. These are connected to grid at the PCC and supplying a nonlinear and unbalanced load. The function of the AVSI is to compensate the reactive, harmonics, and unbalance components in load currents. Here, load currents in three phases are represented by ila, ilb, and ilc, respectively. Also, ig(abc), iμgm(abc), and iμgx(abc) show grid currents, MVSI currents, and AVSI currents in three phases, respectively. The dc link of the AVSI utilizes a split capacitor topology, with two capacitors C1 and C2. The MVSI deliv-ers the available power at distributed energy resource (DER) to grid. The DER can be a dc source or an ac source with rectifier coupled to dc link. Usually, renewable energy sources like fuel cell and PV generate power at variable low dc voltage, while the variable speed wind turbines generate power at variable ac voltage. Therefore, the power generated from these sources use a power conditioning stage before it is con-nected to the input of MVSI. In this study, DER is being represented as a dc source. An inductor filter is used to elim-inate the high-frequency switching components generated due to theswitching of power electronic switches in the inverters [19]. The system considered in this study is assumed to have some amount of feeder resistance R g and inductance Lg . Due to the presence of this feeder impedance, PCC voltage is affected with harmonics [20]. Section III describes the extraction of fundamental positive sequence of PCC voltages and control

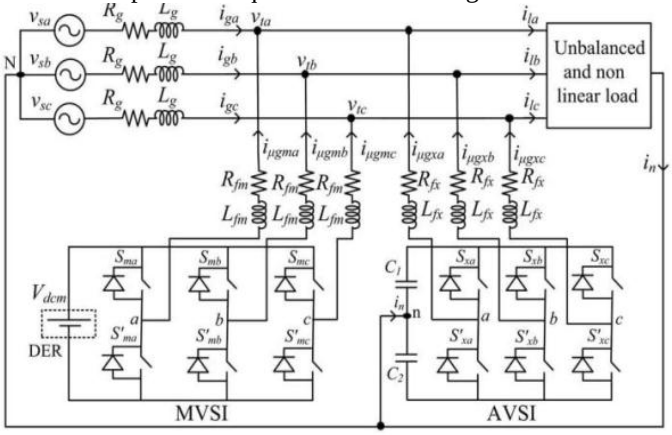

Fig. 1. Topology of proposed DVSI scheme

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strategy for the reference current generation of two inverters in DVSI scheme.

B. Design of DVSI Parameters

1) AVSI: The important parameters of AVSI like dc-link voltage (V_{dc}), dc storage capacitors (C_1 and C_2), interfacing

inductance (L_{fx}), and hysteresis band ($\pm h_x$) are selected based on the design method of split capacitor DSTATCOM topol-ogy [16]. The dc-link voltage across each capacitor is taken as 1.6 times the peak of phase voltage. The total dc-link voltage reference (V_{dcref}) is found to be 1040 V.

Values of dc capacitors of AVSI are chosen based on the change in dc-link voltage during transients. Let total load rating is S kVA. In the worst case, the load power may vary from minimum to maximum, i.e., from 0 to S kVA. AVSI needs to exchange real power during transient to maintain the load power demand. This transfer of real power during the transient will result in deviation of capacitor voltage from its reference value. Assume that the voltage controller takes n cycles, i.e., nT seconds to act, where T is the system time period. Hence, maximum energy exchange by AVSI during transient will be nST . This energy will be equal to change in the capacitor stored energy. Therefore

$$\frac{1}{2}C\left(V_{dcr}^{2} - V_{dc1}^{2}\right) = nST \quad (1)$$

where V_{dcr} and V_{dc1} are the reference dc voltage and maximum permissible dc voltage across C_1 during transient, respectively.

Here, S = 5 kVA, V_{dcr} = 520 V, V_{dc1} = 0.8 $*$ V_{dcr} or 1.2 $*$ V_{dcr}, n = 1, and T = 0.02 s. Substituting these values in (1), the dc-link capacitance (C_1) is calculated to be 2000 µF. Same value of capacitance is selected for C_2.

The interfacing inductance is given by

$$L_{fx} = \frac{1.6\,V_m}{4\,x_{max}}. \quad (2)$$

Assuming a maximum switching frequency (f_{max}) of 10 kHz and hysteresis band (h_x) as 5% of load current (0.5 A), the value of L_{fx} is calculated to be 26 mH.

MVSI: The MVSI uses a three-leg inverter topology. Its dc-link voltage is obtained as 1.15 $*$ V_{ml}, where V_{ml} is the peak value of line voltage. This is calculated to be 648 V. Also, MVSI supplies a balanced sinusoidal current at unity power factor. So, zero sequence switching harmonics will be absent in the output current of MVSI. This reduces the filter requirement for MVSI as compared to AVSI [21]. In this analysis, a filter inductance (Lf m) of 5 mH is used.

C. Advantages of the DVSI Scheme

The various advantages of the proposed DVSI scheme over a single inverter scheme with multifunctional capabilities [7]–

[9] are discussed here as follows:

1) Increased Reliability: DVSI scheme has increased reli-ability, due to the reduction in failure rate of components and the decrease in system down time cost [13]. In this scheme, the total load current is shared between AVSI and MVSI and hence reduces the failure rate of inverter switches. Moreover, if one inverter fails, the other can continue its operation. This reduces the lost energy and hence the down time cost. The reduction in system down time cost improves the reliability.

2) Reduction in Filter Size: In DVSI scheme, the current supplied by each inverter is reduced and hence the current rating of individual filter inductor reduces. This reduction in current rating reduces the filter size. Also, in this scheme, hysteresis current control is used to track the inverter reference currents. As given in (2), the filter inductance is decided by the inverter switching frequency. Since the lower current rated semicon-ductor device can be switched at higher switching frequency, the inductance of the filter can be lowered. This decrease in inductance further reduces the filter size.

3) Improved Flexibility: Both the inverters are fed from separate dc links which allow them to operate independently, thus increasing the flexibility of the system. For instance, if the dc link of the main inverter is disconnected from the system, the load compensation capability of the auxiliary inverter can still be utilized.

4) Better Utilization of Microgrid Power: DVSI scheme helps to utilize full capacity of MVSI to transfer the entire power generated by DG units as real power to ac bus, as there is AVSI for harmonic and reactive power compensation. This increases the active power injection capability of DGs in microgrid [22].

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5) Reduced DC-Link Voltage Rating: Since, MVSI is not delivering zero sequence load current components, a single capacitor three-leg VSI topology can be used. Therefore, the dc-link voltage rating of MVSI is reduced approximately by 38%, as compared to a single inverter system with split capacitor VSI topology.

III. CONTROL STRATEGY FOR DVSI SCHEME

A. Fundamental Voltage Extraction

The control algorithm for reference current generation using ISCT requires balanced sinusoidal PCC voltages. Because of the presence of feeder impedance, PCC voltages are distorted. Therefore, the fundamental positive sequence components of the PCC voltages are extracted for the reference current gen-eration. To convert the distorted PCC voltages to balanced

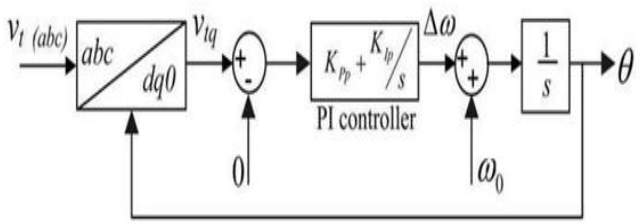

Fig. 2. Schematic diagram of PLL.

sinusoidal voltages, dq0 transformation is used. The PCC volt-ages in natural reference frame (vta, vtb, and v tc) are first

$$\begin{bmatrix} v_{td} \\ v_{tq} \\ v_{t0} \end{bmatrix} = C \begin{bmatrix} v_{ta} \\ v_{tb} \\ v_{tc} \end{bmatrix} \quad (3)$$

$$C = \frac{2}{3}\begin{bmatrix} \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}.$$

transformed into dq0 reference frame as given by

In order to get θ, a modified synchronous reference frame (SRF) phase locked loop (PLL) [23] is used. The schematic diagram of this PLL is shown in Fig. 2. It mainly consists of a pro-portional integral (PI) controller and an integrator. In this PLL, the SRF terminal voltage in q-axis (vtq) is compared with 0 V and the error voltage thus obtained is given to the PI controller. The frequency deviation ω is then added to the reference fre-quency ω0 and finally given to the integrator to get θ. It can be proved that, when, θ = ω0 t and by using the Park's transforma-tion matrix (C), q-axis voltage in dq0 frame becomes zero and hence the PLL will be locked to the reference frequency (ω0). As PCC voltages are distorted, the transformed voltages in dq0 frame (vtd and vtq) contain average and oscillating components of voltages. These can be represented as

$$v_{td} = \bar{v}_{td} + \tilde{v}_{td}, \quad v_{tq} = \bar{v}_{tq} + \tilde{v}_{tq} \quad (4)$$

where vtd and vtq represent the average components of vtd and vtq , respectively. The terms vtd and vtq indicate the oscillating components of vtd and vtq , respectively. Now the fundamental positive sequence of PCC voltages in natural reference frame can be obtained with the help of inverse dq0 transformation as given by

$$\begin{bmatrix} v_{ta+1} \\ v_{tb+1} \end{bmatrix} = C^{I} \begin{bmatrix} \bar{v}_{td} \\ \bar{v}_{tq} \end{bmatrix}. \quad (5)$$

These voltages vta+1, vtb+1, and vtc+1 are used in the reference current generation algorithms, so as to draw balanced sinusoidal currents from the grid.

B. Instantaneous Symmetrical Component Theory

ISCT was developed primarily for unbalanced and nonlinear load compensations by active power filters. The system topol-ogyshown in Fig. 3 is used for realizing the reference current for the compensator [15]. The ISCT for load compensation is derived based on the following three conditions

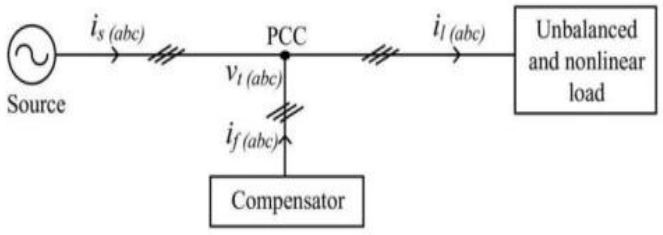

Fig. 3. Schematic of an unbalanced and nonlinear load compensation scheme

1) The source neutral current must be zero. Therefore

$$i_{sa} + i_{sb} + i_{sc} = 0.$$

2) The phase angle between the fundamental positive sequence voltage ($v_{ta\ 1}$) and source current (i_{sa}) is φ

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$\angle v_{ta}^{+}{}_{1} = \angle i_{sa} + \varphi$.

3) The average real power of the load (Pl) should be supplied by the source

$$v_{ta}^{+}{}_{1} i_{sa} + v_{tb}^{+}{}_{1} i_{sb} + v_{tc}^{+}{}_{1} i_{sc} = P_l \quad (8)$$

Solving the above three equations, the reference source currents can be obtained as

$$i_{sa}^{*} = \frac{v_{ta}^{+}{}_{1} + \beta(v_{tb}^{+}{}_{1} - v_{tc}^{+}{}_{1})}{\sum_{j=a,b,c} v_{tj}^{+2}} P_l$$

$$i_{sb}^{*} = \frac{v_{tb}^{+}{}_{1} + \beta(v_{tc}^{+}{}_{1} - v_{ta}^{+}{}_{1})}{\sum_{j=a,b,c} v_{tj}^{+2}} P_l$$

$$i_{sc}^{*} = \frac{v_{tc}^{+}{}_{1} + \beta(v_{ta}^{+}{}_{1} - v_{tb}^{+}{}_{1})}{\sum_{j=a,b,c} v_{tj}^{+2}} P_l$$

where $\beta = \frac{\tan\varphi}{\sqrt{3}}$. The term φ is the desired phase angle between the fundamental positive sequence of PCC voltage and source current. To achieve unity power factor for source current, substitute $\beta = 0$ in (9). Thus, the reference source currents for three phases are given by

$$i_s^{*}(abc) = \frac{v_{t(abc)1}^{+}}{\sum_{j=a,b,c} v_{tj}^{+2}} P_l \quad (10)$$

$$P_l = \frac{1}{T}\int_{t_1-T}^{t_1} (v_{ta}^{+}{}_{1} i_{la} + v_{tb}^{+}{}_{1} i_{lb} + v_{tc}^{+}{}_{1} i_{lc})\, dt \quad (11)$$

where t is any arbitrary time instant. Finally, the reference currents for the compensator can be generated as follows:

$$i_{f^{*}(abc)} = i_{l(abc)} - i_{s^{*}(abc)}. \quad (12)$$

Equation (12) can be used to generate the reference filter currents using ISCT, when the entire load active power, Pl is supplied by the source and load compensation is performed by a single inverter. A modification in the control algorithm is required, when it is used for DVSI scheme. The following section discusses the formulation of control algorithm for DVSI scheme. The source currents, is(abc) and filter currents if (abc) will be equivalently represented as grid currents ig(abc) and AVSI currents I µgx(abc), respectively, in further sections.

C. Control Strategy of DVSI

Control strategy of DVSI is developed in such a way that grid and MVSI together share the active load power, and AVSI (6) supplies rest of the power components demanded by the load.

1) Reference Current Generation for Auxiliary Inverter:

The dc-link voltage of the AVSI should be maintained constant for proper operation of the auxiliary inverter. DC-link voltage

(7) variation occurs in auxiliary inverter due to its switching and ohmic losses. These losses termed as Ploss should also be sup-plied by the grid. An expression for Ploss is derived on the condition that average dc capacitor current is zero to main- tain a constant capacitor voltage [15]. The deviation of average capacitor current from zero will reflect as a change in capaci- tor voltage from a steady state value. A PI controller is used to generate Ploss term as given by

$$P_{loss} = K_{P\,v}\, e_{vdc} + K_{Iv} \int e_{vdc}\, dt \quad (13)$$

where evdc = Vdcref − vdc, vdc represents the actual voltage sensed and updated once in a cycle. In the above equation, KP v and KIv represent the proportional and integral gains of dc-link PI controller, respectively. The Ploss term thus obtained should be supplied by the grid, and therefore AVSI reference currents can be obtained as given in (14). Here, the dc-link voltage PI controller gains are selected so as to ensure stability and better dynamic response during load change [24]

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$$i_{\mu gxa}^{*} = i_{la} - \frac{v_{ta1}^{+}}{\sum_{j=a,b,c} v_{tj}^{+2}}(P_l + P_{loss})$$

$$i_{\mu gxb}^{*} = i_{lb} - \frac{v_{tb}^{+}{}_{1}}{\sum_{j=a,b,c} v_{tj}^{+2}}(P_l + P_{loss}) \qquad (14)$$

$$i_{\mu gxc}^{*} = i_{lc} - \frac{v_{tc1}^{+}}{\sum_{j=a,b,c} v_{tj}^{+2}}(P_l + P_{loss}).$$

2) Reference Current Generation for Main Inverter: The MVSI supplies balanced sinusoidal currents based on the avail- able renewable power at DER. If MVSI losses are neglected, the power injected to grid will be equal to that available at DER (Pμg). The following equation, which is derived from ISCT can be used to generate MVSI reference currents for three phases (a, b, and c

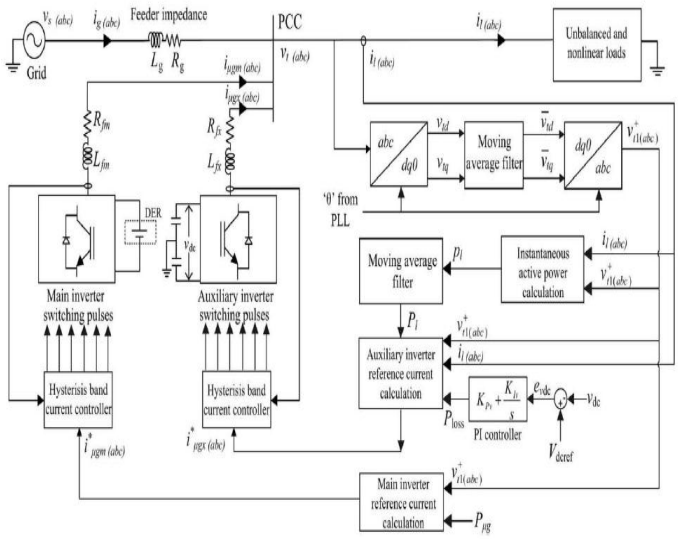

Fig. 4. Schematic diagram showing the control strategy of proposed DVSI scheme.

comparator. This controller has the advantage of peak current limiting capacity, good dynamic response, and simplicity in implementation [14]. A hysteresis controller is a high-gain pro-portional controller. This controller adds certain phase lag in the operation based on the hysteresis band and will not make the system unstable. Also, the proposed DVSI scheme uses a first-order inductor filter which retains the closed-loop system stability [25]. The entire control strategy is schematically repre-sented in Fig. 4. Applying Kirchoff's current law (KCL) at the PCC in Fig. 4

$$i_{\mu gx\,j} = i_{l\,j} - (i_{g\,j} + i_{\mu gm\,j}), \qquad \text{for } j = a,\ b,\ c. \qquad (16)$$

By using (14) and (16), an expression for reference grid current in phase-*a* (*i*∗*ga*) can be obtained as

$$i_{ga}^{*} = \frac{V_{ta\ 1}^{+}}{\sum_{j=a,b,c} v_{tj}^{+2}}[(P_l + P_{loss}) - P_{\mu g}\ ]. \qquad (17)$$

It can be observed that, if the quantity (Pl + Ploss) is greater than Pμg , the term [(Pl + Ploss) − Pμg] will be a positive quan-tity, and i∗ ga will be in phase with vta + 1. This operation can be calledas the grid supporting or grid sharing mode, as the total load power demand is shared between the main inverter and the grid. The term, Ploss is usually very small compared to Pl. On the other hand, if (Pl + Ploss) is less than Pμg , then [(Pl + Ploss) − Pμg] will be a negative quantity, and hence i∗ ga will be in phase opposition with vta + 1. This mode of operation is called the gridn injecting mode, as the excess power is injected to grid.

IV. SIMULATION STUDIES

The simulation model of DVSI scheme shown in Fig. 1 is developed in PSCAD 4.2.1 to evaluate the performance. The simulation parameters of the system are given in Table I. The simulation study demonstrates the grid sharing and grid

Table I
System parameters for simulation study

Parameters	Values
Grid voltage	400 V(L–L)
Fundamental frequency	50 Hz
Feeder impedance	$R_g = 0.5\ \Omega$, $L_g = 1.0$ mH
AVSI	$C_1 = C_2 = 2000\ \mu$F $V_{dcref} = 1040$ V Interfacing inductor, $L_{fx} = 20$ mH Inductor resistance, $R_{fx} = 0.25\ \Omega$ Hysteresis band ($\pm h_x$) = 0.1 A
MVSI	DC-link voltage, $V_{dcm} = 650$ V Interfacing inductor, $L_{fm} = 5$ mH Inductor resistance, $R_{fm} = 0.25\ \Omega$ Hysteresis band ($\pm h_m$) = 0.1 A
Unbalanced linear load	$Z_{la} = 35 + j19\ \Omega$ $Z_{lb} = 30 + j15\ \Omega$ $Z_{lc} = 23 + j12\ \Omega$
Nonlinear load	3 ϕ diode bridge rectifier with DC side current of 3.0 A
DC voltage controller gains	K_{Pv} =10, $K_{Iv} = 0.05$

injecting modes of operation of DVSI scheme in steady state as well as in transient conditions The distorted PCC voltages due to the feeder impedance without DVSI scheme are shown in Fig. 5(a). If these dis-torted voltages are used for the reference current generation of AVSI, the current compensation will not be proper [14]. Therefore, the fundamental positive sequence of voltages is extracted from these distorted voltages using the algorithm explained in

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Section III-A. These extracted voltages are given in Fig. 5(b). These voltages are further used for the generation of inverter reference currents. Fig. 6(a)–(d) represents active power demanded by load (Pl), active power supplied by grid (Pg), active power supplied by MVSI (Pµg), and active power supplied by AVSI (Px), respectively. It can be observed that, from t = 0.1 to 0.4 s, MVSI is generating 4 kW power and the load demand is 6 kW. Therefore, the remaining load active power (2 kW) is drawn from the grid. During this period, the

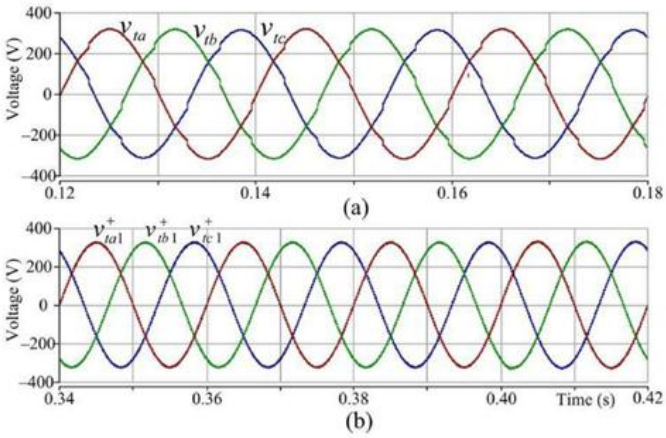

Fig. 5. Without DVSI scheme: (a) PCC voltages and (b) fundamental positive sequence of PCC voltages.

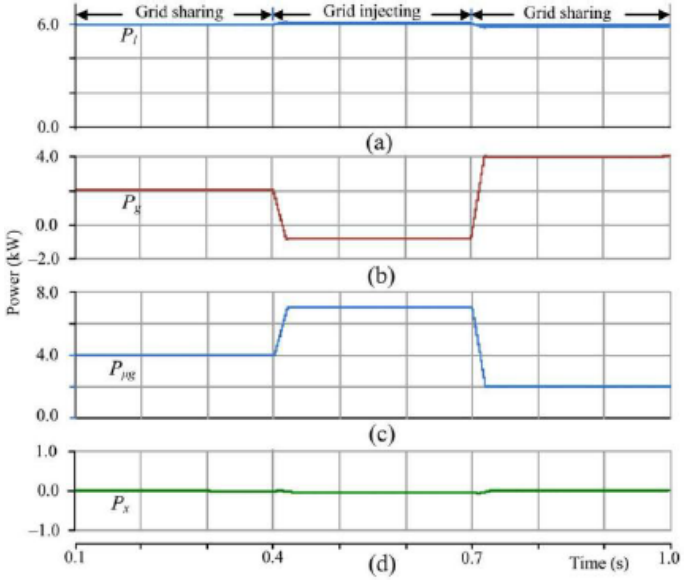

Fig. 6. Active power sharing: (a) load active power; (b) active power supplied by grid; (c) active power supplied by MVSI; and (d) active power supplied by AVSI.

microgrid is operating in grid sharing mode. At t = 0.4 s, the microgrid power is increased to 7 kW, which is more than the load demand of 6 kW. This microgrid power change is considered to show the change of operation of MVSI from grid sharing to grid injecting mode. Now, the excess power of 1 kW is injected to the grid and hence, the power drawn from grid is shown as negative. Fig. 7(a)–(c) shows the load reactive power (Ql), reactive power supplied by AVSI (Qx), and reactive power supplied by MVSI (Qµg), respectively. It shows that total load reactive power is supplied by AVSI, as expected. Fig. 8(a)–(d) shows the plots of load currents (il(abc)), cur rents drawn from grid (ig(abc)), currents drawn from MVSI (iµg(abc)), and currents drawn from the AVSI (iµx(abc)),respectively. The load currents are unbalanced and distorted. The MVSI supplies a balanced and sinusoidal currents duringgrid supporting and grid injecting modes. The currents drawnfrom grid are also perfectly balanced and sinusoidal, as the auxiliary inverter compensates the unbalance and harmonics

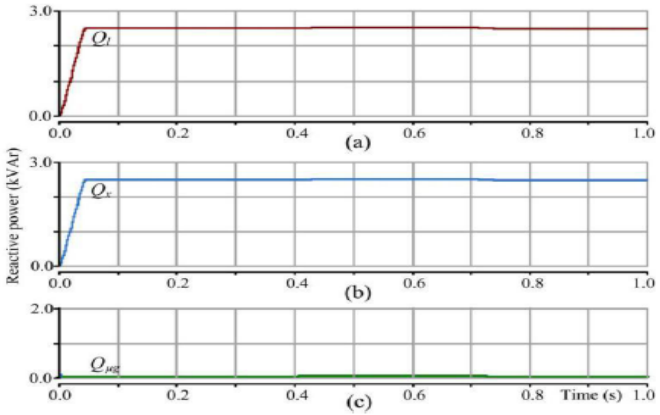

Fig. 7. Reactive power sharing: (a) load reactive power; (b) reactive power supplied by AVSI; and (c) reactive power supplied by MVSI.

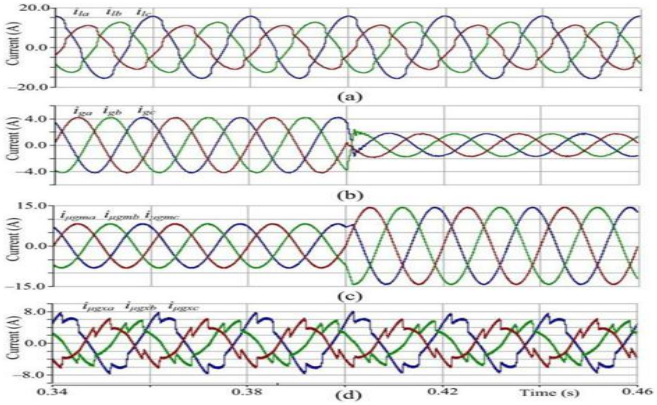

Fig. 8. Simulated performance of DVSI scheme: (a) load currents; (b) grid currents; (c) MVSI currents; and (d) AVSI currents.

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in load currents. Fig. 9(a) shows the plot of fundamental posi-tive sequence of PCC voltage (vta+1) and grid current in phase-a (iga) during grid sharing and grid injecting modes. During grid sharing mode, this PCC voltage and grid current are in phase and during grid injecting mode, they are out of phase. Fig. 9(b) establishes that MVSI current in phase-a is always in phase with fundamental positive sequence of phase-a PCC voltage. The same is true for other two phases. Thus the compensation capability of AVSI makes the source current and MVSI current at unity power factor operation. The dc-link voltage of AVSI

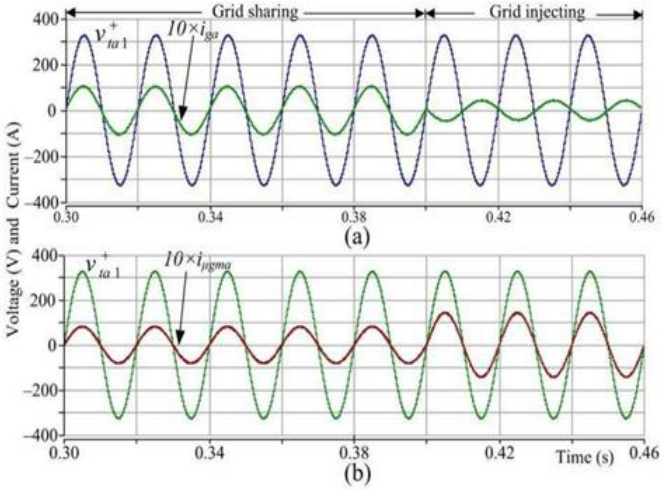

Fig. 9. Grid sharing and grid injecting modes of operation: (a) PCC voltage and grid current (phase-a) and (b) PCC voltage and MVSI current (phase-a).

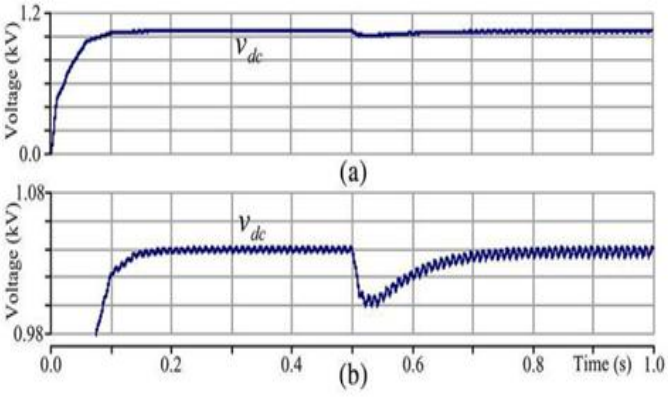

Fig. 11. Experimental setup of DVSI.

is shown in Fig. 10(a) and (b). These figures indicate tha the voltage is maintained constant at a reference voltage (Vdcref) of 1040 V by the PI controller. All these simulation results pre-sented above demonstrate the feasibility of DVSI for the load compensation as well as power injection from DG units in a microgrid.

Table II
System parameters for experimental study

Parameters	Values
Source voltage	50 V L–N (rms), 50 Hz
Feeder impedance	R_g = 0.5 Ω, L_g = 1.0 mH
Reference DC-link voltage of AVSI	V_{dcref} = 220 V
DC-link capacitance of AVSI	$C_1 = C_2 = 4700$ μF
DC-link voltage of MVSI	$V_{dcm} = 150$ V
PI gains of DC-link voltage controller	$K_{Pv} = 80$, $K_{Iv} = 0.08$
Hysterisis band (h)	± 0.15 A
Interfacing inductor (AVSI)	R_{fx}= 0.5 Ω, L_{fx}= 10 mH
Interfacing inductor (MVSI)	R_{fm}= 0.5 Ω, L_{fm}= 5 mH
Unbalanced linear load	$Z_{la} = 24 + j16$ Ω $Z_{lb} = 36 + j16$ Ω $Z_{lc} = 64 + j21$ Ω
Nonlinear load	3 ϕ diode bridge rectifier with a dc current of 2.4 A

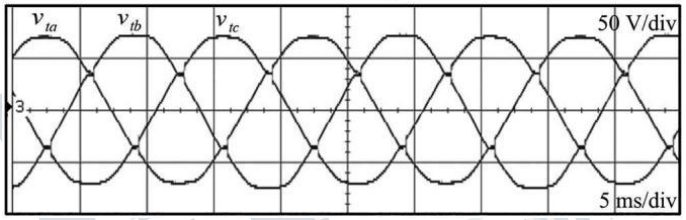

Fig. 12. Experimental results: PCC voltages before compensation.

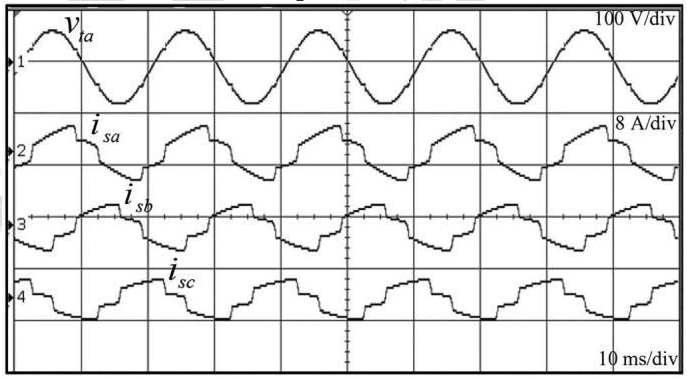

Fig. 13. Experimental results: PCC voltage (phase-a) and grid currents before compensation.

V. EXPERIMENTAL RESULTS

The performance of the proposed DVSI is verified with experimental studies. A digital signal processor (DSP)-based prototype of DVSI as shown in Fig. 11 has been developed in the laboratory. The experimental system parameters are given in Table II. The setup consists of two 10 kVA SEMIKRON build two-level inverter for realizing AVSI and MVSI. A DSP TMS320F28335 is used to process the data in digital domain with a sampling time of 19.5 μs. The signal and logic level circuit consist of Hall effect voltage and current

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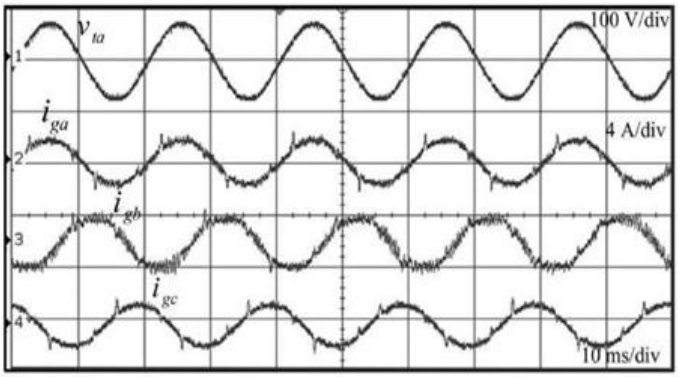
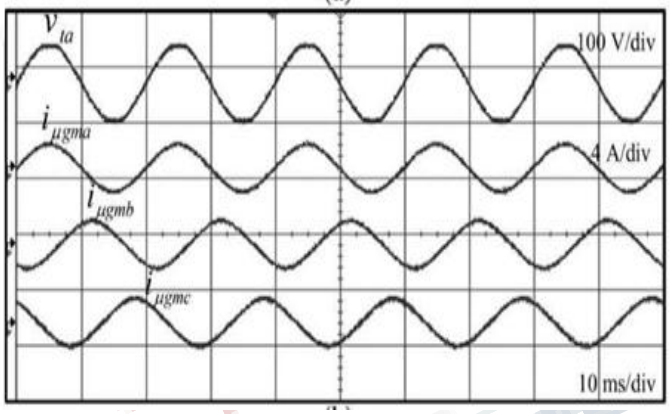
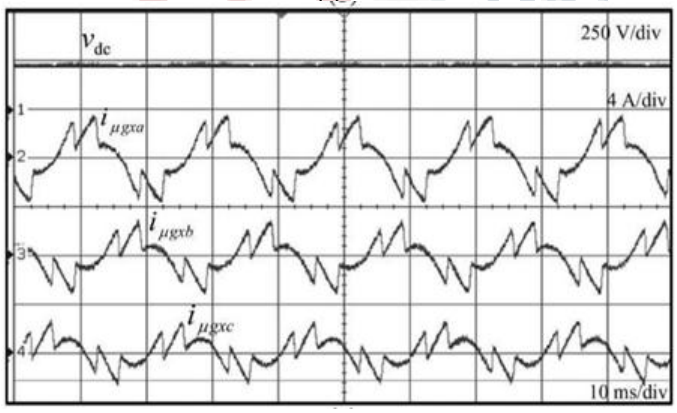
transducers, signal conditioning, and protection circuits along with isolated dc power supplies. A real time algorithm has been implemented in code composer studio (CCS) on the host computer. The DSP acquires the signals and processes them to generate reference currents for AVSI and MVSI. The switching commands gener-ated by the DSP are then issued to inverters through its general purpose input and output ports



(a)



(b)



(c)Fig. 14. Experimental results: (a) PCC voltage (phase-a) and grid currents after compensation; (b) MVSI currents; and (c) dc-link voltage and AVSI currents

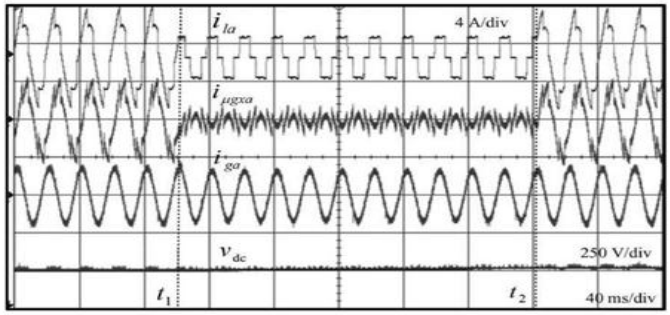


Fig. 15. Experimental results: dynamic performance of AVSI during load change.

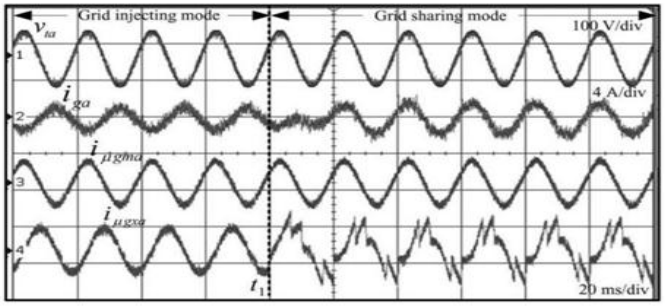


Fig. 16. Experimental results: dynamic performance of DVSI during load change.

The dynamic performance of the AVSI is illustrated by displaying load currents, filter currents, source currents, and dc-link voltage as in Fig. 15. The load changes from unbalanced and nonlinear to balanced nonlinear load at an instant t1. The AVSI begins to compensate the load instantaneously. The grid and filter
currents settle within half a cycle. At the instant t2, the load changes back to its normal value. The source and filter currents again settle within a cycle. The rise and fall in dc-link voltage due to the sudden decrease and increase in load is not visible in the graph. This is because, the dc-link voltage con-trol loop is slow and takes few cycles to settle down. Fig. 16 represents grid current transient during the change of operation of MVSI from grid injecting to grid sharing mode. It is con-sidered that MVSI supplies 300 W during entire operation. A linear unbalanced load which takes an active power of 140 W is supplied by the DVSI
until the time t1. Therefore, the remain-ing microgrid power of
about 160 W is injected to grid. At the instant t1, the load changes to unbalanced and nonlinear which consumes an average power of 500 W. Therefore, beyond t1, an active power of 200 W is supplied from grid. This figure shows that unity power factor for grid current is achieved during grid injecting and grid sharing modes of operation.

VI. CONCLUSION

A DVSI scheme is proposed for microgrid systems with enhanced power quality. Control algorithms are developed to generate reference currents for DVSI using ISCT. The proposed scheme has the capability to exchange power from distributed generators (DGs) and also to compensate the local unbalanced and nonlinear load. The performance of the proposed scheme has been validated through simulation and experimental stud-ies. As compared to a single inverter with multifunctional capabilities, a DVSI has many advantages such as, increased reliability, lower cost due to the reduction in filter size, and more utilization of inverter capacity to inject real power from DGs to microgrid. Moreover, the use of three-phase, three-wire topology for the main inverter reduces the dc-link voltage requirement. Thus, a DVSI scheme is a suitable interfacing option for microgrid supplying sensitive loads.

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