ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

Enhancing the Performance of DSTATCOM in VCM By Designing a Foreign Inductor

[1] Pujari Pavaneshwar, [2] Dr.V.C.Veera Reddy
[1] PG Scholar, [2] Professor
[1] [2] Department of Electrical and Electronics Engineering, Annamacharya Institute of Technology and Sciences, Tirupati, Andhra Pradesh-517507, INDIA

***Abstract*- This paper gives an exhaustive investigation of operation, design and multifunctional control strategy of a Distribution Static Compensator (DSTATCOM) working in voltage control mode (VCM). The dynamic reference load voltage production plan is created as an internal part of the control strategy which enables it to adjust load reactive power in nominal operation, with association provides voltage support during unsettling influences. Additionally an investigation of the voltage regulation capacity of it under different feeder impedances (resistive, inductive) and its nature (strong, weak) is exhibited. This investigation spotlights the limited regulation capability of it in resistive and strong feeder. Also, a design methodology to figure out the estimation of foreign inductor (external to the system) utilized for enhancing the regulation capability of it is exhibited. It is then utilized for load voltage control to exhibit the performance.**

Key words—Distribution static compensator (DSTATCOM), current control, voltage control, power factor, power quality

I. INTRODUCTION

In a Distribution system the switching of large loads and faults in the power system are the cause of voltage disturbances such as dip and swell [1]. Also, in case of radial system, voltage may be distorted or unbalanced of a particular bus if the loads in any section of that system are nonlinear or unbalanced. The loads connected to that bus which are not contributing to the bus voltage pollution are also fed by a set of unbalanced and distorted voltages [12].These issues in the distribution system lead to the poor Power Quality (PQ). The performance of the sensitive loads such as electronic equipments, process-control industries, etc., connected to this type of distribution system are worst affected.

At first, the static var compensator (SCV) was used to compensate reactive current, regulate the load voltage and to improve the transient stability. This SVC caused undesired problems like injection of harmonic current into the system, harmonic amplification and also had a possibility of resonance with the source impedance [2]. Distribution static compensator, DSTATCOM, was proposed as most effective solution for load voltage regulation and also to overcome the issued that rose due to SVC [3],[4].

It supplied fundamental reactive current into source for load voltage regulation [5]. The traditional DSTATCOMs used for voltage regulation were assumed as highly inductive or predominantly large feeder impedance but in a distribution system feeder impedance is resistive in nature [6], [7]. In this condition, DSTATCOM will have a limited or restricted voltage regulation capability [13]. The reference load voltage is taken as 1.0 p.u for voltage regulation application in traditional DSTATCOM [12]. At this load voltage, reactive power is always exchanged by VSI with the source and power factor (pf) retains leading in nature, causes continuous power loss in the feeder and VSI, which is a considerable issue.

Also, a traditional DSTATCOM requires high current rating voltage source inverter (VSI) to provide voltage support [6]. The power rating of the VSI is increased due to this high current requirement as a result it produces more losses in the switches as well as in the feeder. The feeder impedance and its nature (resistive, inductive, strong, and weak) influence the voltage regulation performance of DSTATCOM [13]. The performance of the DSTATCOM based on these is nowhere well defined. The thought of inserting a foreign inductor in line with DSTATCOM operating in VCM or grid connected inverters was proposed for better regulation but only the concept was accounted for it leaving adequate scope for further examination and understanding into the plan points of interest [8],[9].

This paper exhibits the exhaustive investigation of operation and design of a DSTATCOM working in VCM along with the proposed foreign inductor. Also a multifunctional control strategy consisting of a dynamic reference load voltage production plan as an internal part of the control strategy. This strategy enables it to adjust load reactive power in nominal operation and provides voltage support during unsettling influences. Additionally an investigation of the voltage regulation capacity of it under different feeder impedances (resistive, inductive) and its nature (strong, weak) is carried out. This

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

investigation spotlights the limited regulation capability of it in resistive and strong feeder. Also, a design methodology to figure out the estimation of foreign inductor (external to the system) utilized for enhancing the regulation capability of it is exhibited. It is then utilized for load voltage control to exhibit the performance.

II. DSTATCOM TOPOLOGY IN DISTRIBUTION SYSTEM

Consider the three-phase, four-wire radial system shown in Fig. 1(a). Let us select bus 4 as target bus for voltage regulation. The single-phase Thevenin equivalent of the system is shown in Fig. 1(b). Here v_S is the source voltage, R_S is Thevenin equivalent resistance, and L_S is Thevenin equivalent impedance at bus 4.

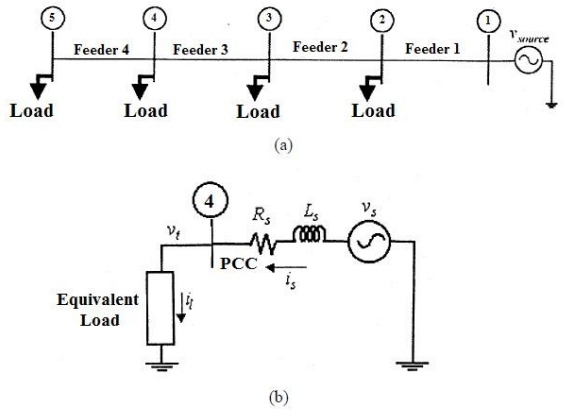

Fig. 1: (a) Radial system under test and (b) its Thevenin equivalent at bus 4.

Fig. 2 shows the equivalent diagram of the DSTATCOM topology connected in distribution system. L_S is source inductance and R_S is source resistance as mentioned in Fig. 1(b). The equivalent load at bus 4 is taken as a nonlinear and unbalanced. A foreign inductor, L_{ext} is incorporated into arrangement amongst load and source points. This inductor causes DSTATCOM to accomplish voltage regulation even in most degraded system conditions, i.e., resistive or strong grid. From IEEE-519 standard, point of common coupling (PCC) ought to be the point which is available to both the utility and the client for direct estimation [10]. Consequently, the PCC is the point where L_{ext} is associated with the source. The DSTATCOM is associated at the point where load and L_{ext} are associated. The DSTATCOM utilizes a three-phase four-wire VSI. An inactive LC filter is associated in each phase to filter high frequency switching segments. Voltages over dc capacitors, V_{dc1} and V_{dc2}, are kept up at a reference estimation of V_{dcref}.

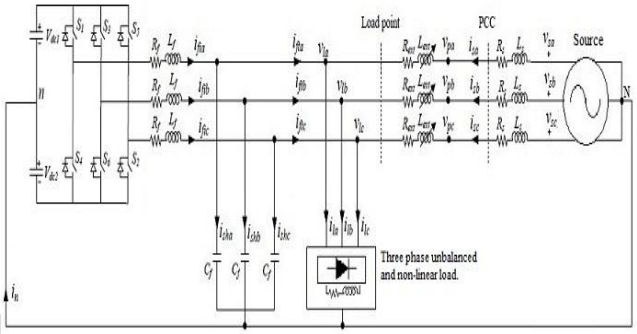

Fig. 2: Three phase equivalent circuit of DSTATCOM topology in distribution system.

III. EFFECT OF FEEDER IMPEDANCE ON VOLTAGE REGULATION

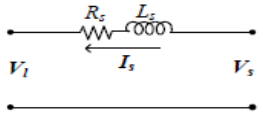

Fig. 3: Equivalent source-load model without considering foreign inductor

To show the impact of feeder impedance on voltage control execution, a proportionate source-regulation show without considering foreign inductor is appeared in Fig. 3. The current in the circuit is given as

$$I_s = \frac{V_S - V_l}{Z_s} \quad (1)$$

where $V_s = V_s\angle\delta$, $V_l = V_l\angle 0$, $I_s = I_s\angle\varphi$, and $Z_s = Z_s\angle\theta_s$, with V_s, V_l, I_s, Z_s, δ, φ, and θ_s are rms source voltage, rms load voltage, rms source current, feeder impedance, load angle, power factor angle, and feeder impedance angle, respectively. The three phase average load power (P_l) is expressed as

$$P_l = \text{Real}\,[3\,V_l \times I_s^*] \quad (2)$$

Substituting V_l and I_S in (2), the load active power is

$$P_l = \frac{3V_l^2}{Z_s}\left[\frac{V_l}{V_s}cos(\theta_s - \delta) - cos\theta_s\right] \quad (3)$$

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

Rearranging (4) for δ

$$\delta = \theta_s - cos^{-1}\left[\frac{V_l}{V_s} cos\left(\theta_s + \frac{P_l Z_s}{3V_l^2}\right)\right] \quad (4)$$

For power exchange from source to load with stable operation in an inductive feeder, additionally, every one of the terms of the second piece of (4), i.e., inside $\cos^{-1}$, are amplitude and also positive. Along these lines, estimation of the second part will be between '0^0' to '90^0' for the whole operation of the load. Therefore, the load point will lie between θ_s to (θ_s - 90^0) under any load operation, and in this manner, greatest conceivable load point is θ_s. The vector expression for source voltage is given as

$$V_s = V_l + I_s Z_s \angle(\theta_s - \varphi) \quad (5)$$

A DSTATCOM directs the load voltage by infusing fundamental reactive current.

The DSTATCOM voltage regulation capacity at various supply voltages for diverse Rs/Xs, vector diagram utilizing (5) are drafted in Fig. 4. To draw these, load voltage magnitude V_l is taken as reference phasor OA having the unity esteem (.i.e. 1.0 p.u.). With point of making $V_l = V_S = 1.0$ p .u., locus of V_S will be a half circle of range V_l. Since, the greatest conceivable load edge is 90^0 in an inductive feeder, phasor Vs can be anyplace inside bend OACBO. It can be seen that the estimation of $\theta_s + \varphi$ must be more prominent than 90^0 for zero voltage control. Furthermore, it is conceivable just when power element is driving at the load terminal as θ_s can't be more than 90^0.

Fig. 4(a) demonstrates the restricting situation when $R_s / X_s = 1$, i.e., $\theta_s = 45^0$. From (4), the maximum possible load angle is 45^0. The maximum value of angle, $\theta_s + \varphi$, can be 135^0 when φ is 90^0. Hence, the limiting source current phasor OE, which is denoted by I_{slimit}, will lead the load voltage by 90^0. Lines OC and AB demonstrate the constraining vectors of V_s and $I_S Z_S$, respectively with D as the crossing point. Subsequently, range under ACDA demonstrates the working district of DSTATCOM for voltage control. The point D has a constraining estimation of $V_{Slimit} = I_S Z_S = 0.706$ p .u. In this way, greatest conceivable voltage control is 29.4%. But, it is difficult to accomplish these two breaking points all the while as δ and φ can't be most extreme at a similar time. Again if Z_S is low at that point source current, which will be practically inductive, will be sufficient to be acknowledged by a DSTATCOM.

Fig. 4(b) considers situation when $R_S/X_S = \sqrt{3}$ i.e., $\theta_s = 30^0$ .The region under ACDA recoils, which demonstrates that with the expansion in R_S/X_S from the restricting quality, the voltage regulation ability diminishes. For this situation the constraining esteems of V_{Slimit} and $I_S Z_S$ are observed to be 0.866 and 0.5 p.u., separately. Here, greatest conceivable voltage regulation is 13.4%.

Anyhow, because of high current prerequisite, a traditional DSTATCOM can give little voltage control. Voltage control execution bends for more resistive feeder, i.e., $\theta_s = 15^0$ as appeared in Fig. 4(c), can be drawn likewise. Here, range under ACDA is immaterial. For this case, barely any voltage regulation is conceivable. In this manner, more the feeder is resistive in nature, lesser will be the voltage regulation ability. Consequently, it is gathered that the voltage regulation capacity of DSTATCOM in a distribution system mostly relies on the feeder impedance.

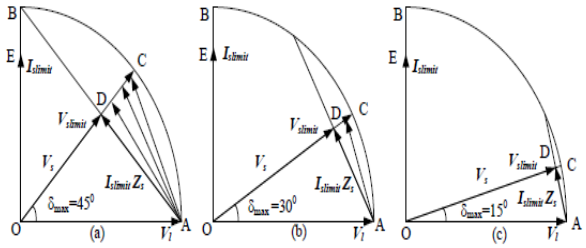

Fig. 4: Voltage regulation performance curve of DSTATCOM at different Rs/Xs. (a) For Rs/Xs = 1. (b) For Rs/Xs =$\sqrt{3}$. (c) For Rs/Xs = 3.73

Due to resistive nature of feeder in a distribution system, DSTATCOM voltage regulation ability is restricted. In addition, high current is required to alleviate little voltage unsettling influences which brings about higher rating of IGBT switches and also expanded misfortunes. One more point worth to be noted is that, in the resistive feeder, there will be some voltage drop in the line at ostensible source voltage which the DSTATCOM may not be capable to compensate to look after load voltage at 1.0 p.u. indeed, even with a perfect VSI.

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

IV. DESIGNING OF FOREIGN INDUCTOR FOR PERFORMANCE ENHANCEMENT AND RATING REDUCTION

This segment exhibits a summed up system to choose foreign inductor for development in DSTATCOM voltage control ability while lessening the present rating of VSI. Fig. 4 indicates single stage comparable DSTATCOM circuit design in distribution system. With adjusted voltages, source current will be

$$I_s = \frac{V_s\angle\delta - V_l\angle 0}{(R_s+R_{ext})+j(X_s+X_{ext})} = \frac{V_s\angle\delta - V_l\angle 0}{R_{sef}+jX_{sef}} \quad (6)$$

where $R_{sef} = R_s+R_{ext}$ and $X_{sef} = X_s+X_{ext}$ are effective feeder resistance and reactance, respectively. Rext is equivalent series resistance (ESR) of foreign inductor, and will be small. With $\theta_{sef} = tan^{-1}\frac{X_{sef}}{R_{sef}}$ and $Z_{sef} = \sqrt{R_{sef}^2 + X_{sef}^2}$ as effective impedance angle and effective feeder impedance, respectively, the imaginary component of I_S is given as effective impedance angle and effective feeder impedance, respectively, the imaginary component of I_s is given as

$$I_s^{im} = \frac{V_s sin\theta_{sef} - V_l \sin(\delta - \theta_{sef})}{Z_{sef}} \quad (7)$$

With the addition of foreign impedance, the effective feeder impedance becomes predominantly inductive. Hence, $Z_{sef} \approx X_{sef}$. Therefore, approximated Iims will be

$$I_s^{im} = \frac{V_s sin\theta_{sef} - V_l \sin(\delta - \theta_{sef})}{X_{sef}} \quad (8)$$

DSTATCOM Power rating (S_{vsi}) is given as follows [21]:

$$S_{vsi} = \sqrt{3}\frac{V_{dc}}{\sqrt{2}} I_{vsi} \quad (9)$$

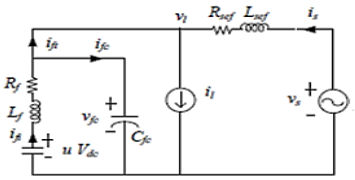

Fig. 5: Single phase equivalent circuit of DSTATCOM topology with foreign inductor in distribution system.

This area exhibits a summed up methodology to choose foreign inductor for development in DSTATCOM voltage regulation ability while lessening the present rating of VSI. Fig. 5 demonstrates single line DSTATCOM circuit graph in distribution system. With adjusted voltages, source current will be compensator current used for voltage regulation (same as I_s^{im}) is obtained by subtracting I_l^{im} from I_{vsi} and given as follows

$$I_s^{im} = I_{vsi} - I_l^{im} = \frac{\sqrt{2}S_{vsi}}{\sqrt{3}V_{dc}} - I_l^{im} \quad (10)$$

Comparing (8) and (10) while using value of δ from (4), following expression is obtained

$$X_{sef} = \frac{V_l sin\theta_{sef} - V_s sin\left[cos^{-1}\left[\frac{V_l}{V_s}\left(cos\theta_{sef} + \frac{P_l Z_{sef}}{3V_l^2}\right)\right]\right]}{\frac{\sqrt{2}S_{vsi}}{\sqrt{3}V_{dc}} - I_l^{im}} \quad (11)$$

The above expression is utilized to process the estimation of foreign inductor. However this foreign inductor has significance during the voltage misfortunes i.e. dip or sag only. Further if this inductor stays connected throughout the operation i.e. even after clearance of misfortune, then there is a continuous voltage drop occurring across it. Hence to overcome this misfortune the foreign inductor designed should be capable to vary its inductance depending upon the voltage misfortune (dip/swell).The mathematical modeling of the same is as provided in the following part. The foreign variable inductor is realized based on the Faraday's law and Lenz's law. The Lenz's law is defined as "A changing electric current through a circuit that contains inductance induces a proportional voltage, which opposes the change in current."By the Faraday's law the following relation is derived

$$V(t) = L_{ext}\frac{di}{dt} \quad (12)$$

By rearranging the above equation we get,

$$I(t)\frac{1}{L_{ext}}\int V(t) \quad (13)$$

The current I(t) is the inductor current flows through the terminals of the foreign inductor. The V(t), measured is equal to voltage across the terminals of the inductor(.i.e.= |Vl –Vpcc|).The inductance depends upon the voltage across its terminals in the system. Hence,

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

during disturbance in the system it responds according to the voltage disturbance. During normal operation the |Vl – Vpcc| approximately equal to zero /very less inductance is observed across the terminals.

A. Analysis of Model

According to the Faraday's law

$$I_{Lext}(\omega t)\frac{1}{L_{ext}}\int V(\omega t).d\,\omega t \quad (14)$$

Now substituting the values in (13), we get

$$I_{Lext}(\omega t)\frac{1}{L_{ext}}\int V_m \sin\omega t\,.d\,\omega t \quad (15)$$

$$I_{Lext}(\omega t) = -\frac{V_m}{L_{ext}}\cos\omega t \quad (16)$$

The (16) can be rewritten as

$$I_{Lext}(\omega t) = -\frac{V_m}{L_{ext}}\sin(90^0 - \omega t) \quad (17)$$

The (17) satisfies the Lenz's law. Also it can be observed that the flowing current,I_{Lext}, lags the voltage causing it to flow. Hence, the model verifies the inductive nature and change in voltage leads to change in inductor current, so it also has variable inductance nature.

V. STUDY OF DSTATCOM WITH DESIGNED FOREIGN INDUCTOR

Here, it is expected that the considered DSTATCOM ensures load voltage regulation dip of 60%. Thus, source voltage V_s = 0.6 p.u. is considered as most pessimistic scenario voltage unsettling influences. During voltage unsettling influences, the loads ought to stay operational while enhancing the DSTATCOM capacity to alleviate the list. In this way, the load voltage during voltage dip is kept up at 0.9 p.u., which is adequate for tasteful operation of the load. In the present case, greatest required estimation of I_l^{im} is 10 A. With the system parameters mentioned in the Simulink model , the reactance in the wake of understanding (11) is observed to be 2.2 (Lsef = 7 mH). Subsequently, estimation of foreign inductance, Lext, will be 6.7 mH. This foreign inductor is chosen while fulfilling the limitations, for example, greatest load control request, rating of DSTATCOM, and measure of dip to be relieved. In this design case, for base voltage and base power rating of 400 V and 10 kVA, separately, the estimation of foreign inductance is 0.13 p.u. Besides, with aggregate inductance of 7 mH (foreign and furthermore, real system inductance), the aggregate impedance will be 0.137 p. u. The short out limit of the line will be 1/0.13 = 7.7 p.u. which is adequate for the tasteful operation of the system. Moreover, an originator dependably has adaptability to discover reasonable estimation of L_{ext} if the limitations are changed or circuit conditions are changed. Besides, ordinary DSTATCOM worked for accomplishing voltage regulation utilizes substantial feeder inductances [6], [7].

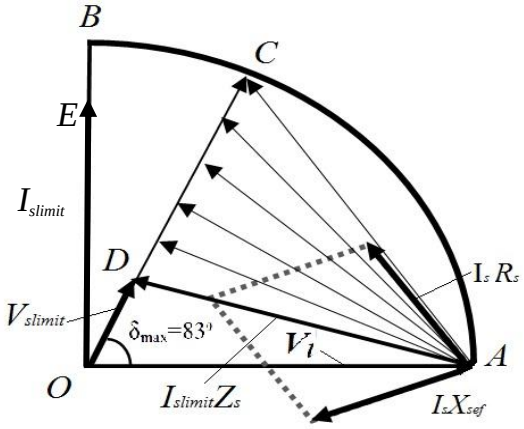

Fig. 6: Voltage regulation performance of DSTATCOM with foreign inductance.

With the foreign inductance while disregarding its ESR, Rs/Xsef will be 0.13 i.e., θ_{sef} = 83°. Voltage control execution bends of the DSTATCOM for this situation are appeared in Fig. 6, where the zone under ACDA covers the larger part of the stable working reach OABO. Henceforth, presentation of foreign inductor incredibly enhances the DSTATCOM voltage control capacity. Also, because of expanded successful feeder impedance the present prerequisite for dip alleviation likewise diminishes. Additionally, if ESR of the foreign inductor is included, at that point the proportionate feeder impedance edge changes marginally (i.e., from 83° to 80.45°), and has insignificant impact on the expression gotten in (11) and also on the voltage control ability of the DSTATCOM.

VI. MULTIFUNCTIONAL CONTROL STRATEGY

This part shows a multifunctional control strategy to move forward the execution of DSTATCOM with

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

association of the foreign inductor Lext. Right off the bat, a dynamic reference voltage regulation based on the planned control of the load basic current, PCC voltage, and voltage over the foreign inductor is figured. At that point, a proportional integral (PI) controller is utilized to control the load angle which helps in managing the dc bus voltage at reference esteem. At last, three stage reference voltage estimations are created. The pictorial representation of the control procedure is demonstrated in Fig. 7.

A. *Derivation of Dynamic Reference Voltage Magnitude (V_l^*)*

In traditional DSTATCOM operating in VCM, the reference Voltage estimation is kept up at a consistent estimation of 1.0 p.u. Source currents can't be controlled in this reference generation plan. Along these lines, control element will not be stable and source trades reactive power with the system even at ostensible supply. To beat this constraint, a multifunctional control procedure is created to produce reference load voltage. This strategy allows DSTATCOM to set different reference voltages during various operating conditions. The strategy is described in the following

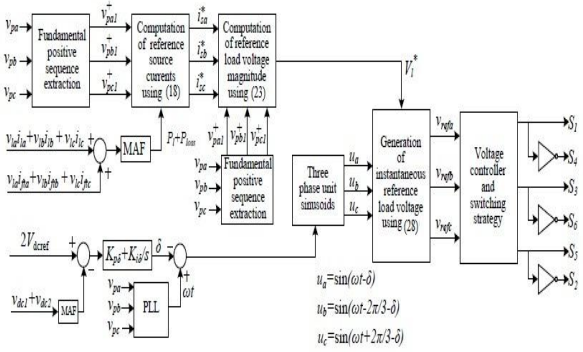

Fig. 7: Block diagram of proposed multifunctional control strategy

1) Normal Operation*:* It is characterized as the condition when Voltage regulation lies between 0.9 to 1.1 p.u. For this situation, the proposed multifunctional control strategy controls voltage estimation such that the source currents are adjusted sinusoidal and VSI does not trade any reactive power with the source. Subsequently, the source supplies just fundamental positive sequence current segment to support the normal load power and VSI misfortunes. Reference source current i_{sj}^* (where j = a; b; c are three phases), registered utilizing momentary symmetrical segment hypothesis, are given as

$$I_{sj}^* = \frac{v_{lj1}^+}{\Delta_1^+}\left(P_{lavg} - P_{loss}\right) \quad (18)$$

where, $\Delta_1^+ = \sum_{j=a,b,c}\left(v_{lj1}^+\right)^2$, the voltages v_{la1}^+,v_{lb1}^+, and v_{lc1}^+ are fundamental positive sequence components of PCC voltages, P_{lavg} is average load power and P_{loss} is VSI losses . P_{lavg} and P_{loss}, are calculated using moving average filter (MAF) as follows:

$$P_{lavg} = \frac{1}{T}\int_{t_1}^{t_1+T}(v_{la}i_{la} + v_{lb}i_{lb} + v_{lc}i_{lc})dt \quad (19)$$

$$P_{loss} = \frac{1}{T}\int_{t_1}^{t_1+T}\left(v_{la}i_{fta} + v_{lb}i_{ftb} + v_{lc}i_{ftc}\right)dt \quad (20)$$

The reference source currents must be in phase with the respective phase fundamental positive sequence PCC voltages for achieving UPF at the PCC. Instantaneous PCC voltage and reference source current in phase-a can be defined as follows:

$$v_{ta1}^+ = \sqrt{2}V_{ta1}^+ \sin(\omega t - \varphi_{ta1}^+),$$
$$i_{sa}^* = \sqrt{2}I_{sa}^* \sin(\omega t - \varphi_{ta1}^+) \quad (21)$$

where V_{ta1}^+ and φ_{ta1}^+pa1 are rms voltage and angle of fundamental positive sequence voltage in phase-a, respectively. I_{sa}^* is the rms reference source current obtained from (18). With foreign impedance, the expected load voltage is given as follows:

$$\bar{V}_{la} = \bar{V}_{pa1}^+ - \bar{I}_{sa}^* Z_{ext} \quad (22)$$

From (21) and (22), the load voltage magnitude will be

$$V_{la} = \sqrt{\begin{matrix}[(V_{ta1}^+ cos\varphi_{ta1}^+ - I_{sa}^* \sin(\theta_{ext} - \varphi_{ta1}^+))^2 + \\ (V_{ta1}^+ sin\varphi_{ta1}^+ - I_{sa}^* \cos(\theta_{ext} - \varphi_{ta1}^+))^2]\end{matrix}} \quad (23)$$

ith UPF at the PCC, the voltage over the foreign inductor will lead the PCC voltage by 90^0. Ignoring ESR of foreign inductor, it can be watched that the voltage over Foreign inductor enhances the load voltage contrasted with the PCC voltage. This highlights another favorable position of foreign inductor where it helps in enhancing the load

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

voltage. As long as V_{la} lies between 0.9 to 1.1 p.u., same voltage is utilized as reference terminal voltage (V_l^*), i.e.,

$$\text{if } V_{la} \in [0.9 - 1.1 \text{ p.u.}] \text{ , then } V_l^* = V_{la}. \quad (24)$$

2) Operation during Dip: Voltage dip is considered when value of (17) is less than 0.9 p.u. To keep filter current minimum, the reference voltage is set to 0.9 p.u. Therefore,

$$V_l^* = 0{:}9 \text{ p.u.} \quad (25)$$

3) Operation during Swell: A voltage swell is considered when any of the PCC phase voltage exceeds 1.1 p.u. In this case, reference load voltage (V_l) is set to 1.1 p.u. which results in minimum current injection. Therefore,

$$V_l^* = 1{:}1 \text{ p.u.} \quad (26)$$

B. Calculation of Load Angle (δ)

Normal real power at the PCC (P_{pcc}) is total of normal load power (P_l) and VSI misfortunes (P_{loss}). The real power Ppcc is taken from the source contingent on the point between source and load voltages, i.e., load angle δ. In the event that DSTATCOM dc bus capacitor voltage is directed to reference esteem, at that point in consistent state condition P_{loss} is a steady esteem and structures a small amount of P_{pcc}. Thus, δ is likewise a steady esteem. The dc link voltage is directed by producing a reasonable estimation of δ. The normal voltage crosswise over dc capacitors (V_{dc1} + V_{dc2}) is contrasted and a reference voltage and blunder is passed through a PI controller. Yield of PI controller δ , is given as

$$\delta = K_{p\delta} e_{vdc} + K_{i\delta} \int e_{vdc} dt \quad (27)$$

$e_{vdc} = 2V_{dcref} - (V_{dc1} + V_{dc2})$ is the voltage error. K_p and K_i are proportional and integral amplifiers, individually.

C.Generation of Instantaneous Reference Voltage

Choosing appropriate reference regulation voltage magnitude and processing load point from (27), the three phase adjusted sinusoidal reference load voltages are given as takes after:

$$v_{refa} = \sqrt{2} V_l^* \sin(\omega t - \delta);$$

$$v_{refb} = \sqrt{2} V_l^* \sin(\omega t - 2\pi/3 - \delta);$$

$$v_{refc} = \sqrt{2} V_l^* \sin(\omega t + 2\pi/3 - \delta) \quad (28)$$

These voltages are realized by the VSI using a predictive voltage controller.

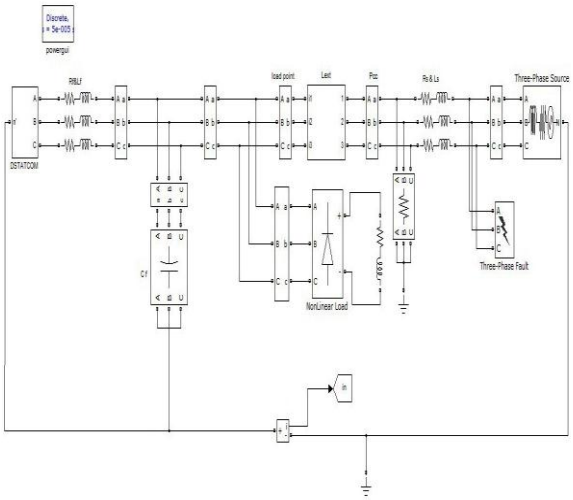

Fig. 8: Simulink Models of distribution system with DSTATCOM and proposed foreign inductor

VII. SIMULATION RESULTS

The Simulink models of the proposed foreign inductor and the DSTATCOM in distribution system are shown in the Fig.8. In this the system has one three phase source which supplies 230 V (rms L-N) at 50Hz feeding a three phase rectifier supplying R-L load of 50 Ω and 200 mH acting as nonlinear load. The feeder resistance and inductance are 0.3Ω and 0.3mH respectively.

The DSTATCOM has a power rating of 30kVA with DC-link voltage of 520 V across each capacitor of 2600 µF rating. The system is provided with a passive LC filter whose L and C ratings are 5 mH and 20 µF respectively. Here the proposed foreign inductor is placed in line with the source and load i.e. at the point of common coupling (PCC). The voltage dip and swell are simulated by assigning appropriate values to the *Three Phase Fault* block. The inputs to this block control the magnitude and timing of voltage dip and swell.

The traditional DSTATCOM steady state waveforms of three phase PCC voltages, load voltages, source currents, filter currents, and load currents are shown in Fig. 9(a)-(e), respectively with resistive and strong feeder. It has to compensate only for feeder drop but, from the

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

load voltage waveform shown in Fig. 9(b) depicts that the voltage magnitude is 225V. Hence, it has limited voltage regulation capability in a resistive feeder. An observation can be made from Fig. 9(c) source current is massive and nearly leading load voltage by 90°.This massive reactive current is supplied by the VSI, as shown in Fig. 9(d), this maximize its rating. These outcomes affirm that DSTATCOM requires large current rating VSI even for smaller voltage regulation and also it can't provide voltage regulation in resistive feeder. The high current causes extra losses in the system.

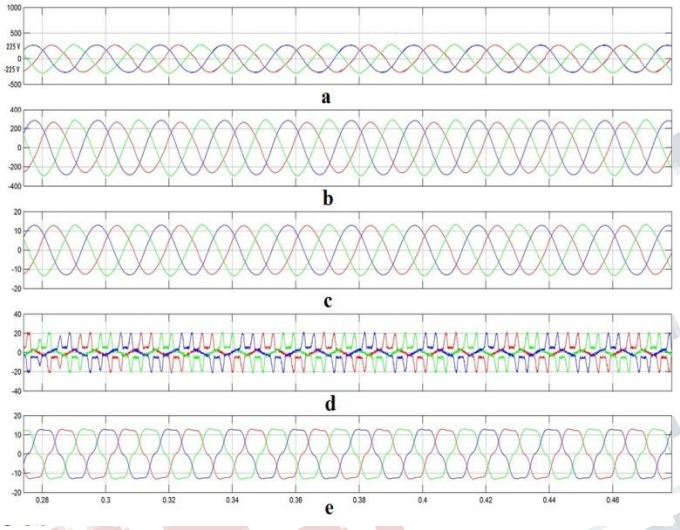

Fig. 9: Voltage regulation performance of traditional DSTATCOM with resistive feeder.
(a) PCC voltages."V" (b) Load Voltages. "V" (c) Source currents. "A" (d) Filter currents. "A" (e) Load currents. "A"

Fig.10(a)-(e) provide the steady state waveforms with the designed foreign inductance and multifunctional control strategy. This plan simultaneously controls load voltages and source currents. The three phase normal PCC voltages are shown in Fig. 10(a).The load voltages and source currents waveforms are shown in Fig. 10(b) and (c), respectively. These waveforms are balanced and sinusoidal. Also, UPF is achieved at the PCC. Hence, compensator supplies only load harmonic and reactive power in addition to reactive power requirement of the L_{ext}. The THDs in the load currents are 12.13%, 10.73% and 11.71% for phases a; b; and c, respectively. After the compensation, the THDs in source currents are reduced to 1.32%, 1.13%and 1.46%, respectively in phases a; b; and c .The filter and load currents are shown in Fig.10 (d) and (e).

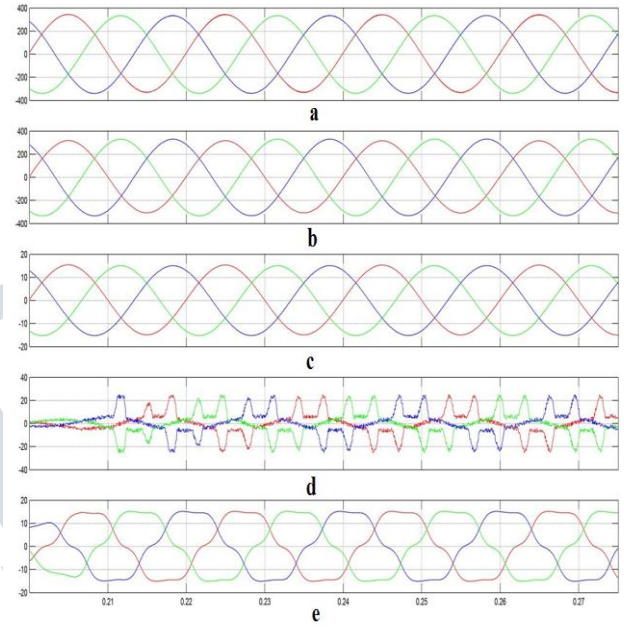

Fig. 10: Performance of DSTATCOM during normal operation with proposed plan.
(a) PCC voltages."V" (b) Load Voltages. "V" (c) Source currents. "A" (d) Filter currents. "A" (e) Load currents. "A"

A. DURING VOLTAGE DIP

Fig. 11(a) shows the PCC voltages. Control of reference load voltage based on the coordinated control of fundamental load current, PCC voltage, and voltage across the foreign inductor allows DSTATCOM to set different constant reference voltage. The proposed plan detects voltage dip and load voltage is changed to 0.9p.u. The waveforms of load voltages are shown in Fig. 11(b). This guarantees continuous, flexible, and robust operation of the load. The source currents are increased during dip period as demonstrated in Fig. 11(c). Fig. 11(d) shows the filter currents which increase during dip period to support the load voltage. The load currents waveforms are

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

presented in Fig. 11(e) are nearly constant during entire operation. Once the dip is removed, slowly all the waveforms reach the pre-dip values. With the outcomes of Fig. 11(a)-(e), it can be concluded that the proposed plan makes load operation continuous.

B.DURING VOLTAGE SWELL

The PCC voltages are shown in Fig. 12(a). The algorithm detects swell and maintains load voltage at 1.1 p.u. The waveforms are shown in Fig. 12(b). The waveforms of the source, filter, and load currents are shown in Fig. 12(c)-(e), respectively. The filter currents increase during swell which increases the source currents as well. Load currents are nearly constant throughout the operation. Once swell is removed, it is detected by the control strategy and system is brought to the steady state conditions. It confirms effectiveness of the proposed plan.

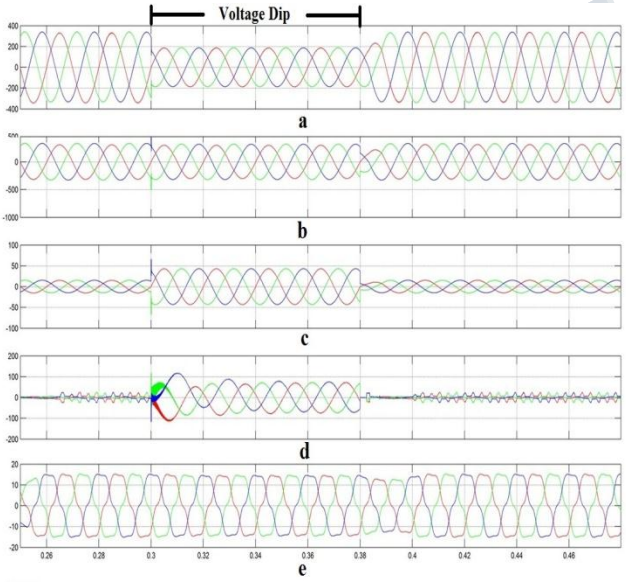

Fig. 11: Voltage regulation performances of DSTATCOM during voltage dip with proposed plan. (a) PCC voltages."V" (b) Load Voltages. "V" (c) Source currents. "A" (d) Filter currents. "A" (e) Load currents. "A"

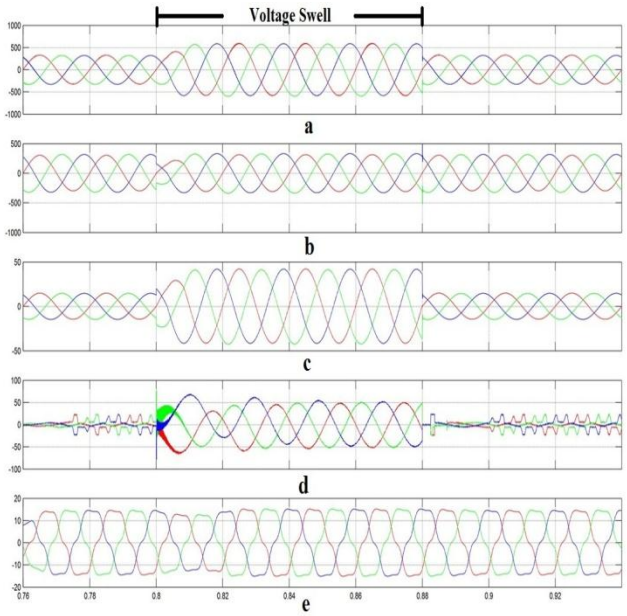

Fig. 12: Voltage regulation performances of DSTATCOM during voltage swell with proposed plan. (a) PCC voltages."V" (b) Load Voltages. "V" (c) Source currents. "A" (d) Filter currents. "A" (e) Load currents. "A"

CONCLUSION

This paper has provided an investigation about the operation and voltage control capacity under different feeder situations of a DSTATCOM working in voltage control mode. This investigation spotlights the fact that it has limited voltage regulation capability in resistive and strong feeder situation. An outline methodology for choosing appropriate estimation of foreign inductor used to enhance regulation capability is given. The foreign inductor is an exceptionally basic and inexpensive arrangement for enhancing the voltage regulation.The proposed arrangement exhibit better regulation capability, a reduction in current rating of VSI, lessened misfortunes in the VSI and feeder. This plan also ensured unity power factor (UPF) operation during nominal operation and maintained load voltage constant during voltage misfortunes.

Additionally, the internal part of multifunctional control strategy, dynamic reference voltage magnitude generation plan enables DSTATCOM to set diverse steady reference voltage during voltage unsettling

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

influences. Simulation outcomes approve the adequacy of the proposed arrangement.

REFERENCES

[1] M. H. Bollen, Understanding power quality problems. vol. 3, IEEE press New York, 2000.
[2] S. Ostroznik, P. Bajec, and P. Zajec, "A study of a hybrid filter," IEEE Trans. Ind. Electron., vol. 57, no. 3, pp. 935–942, Mar. 2010.
[3]C. Kumar and M. Mishra, "A voltage-controlled DSTATCOM for powerquality improvement," IEEE Trans. Power Del., vol. 29, no. 3, pp. 1499–1507, June 2014.
[4]S. Narula, B. Singh, and G. Bhuvaneswari, "Improved power-qualitybased welding power supply with overcurrent handling capability," IEEE Trans. Power Electron., vol. 31, no. 4, pp. 2850–2859, April 2016.
[5]T. Aziz, M. Hossain, T. Saha, and N. Mithulananthan, "VAR planning with tuning of STATCOM in a DG integrated industrial system," IEEE Trans. Power Del., vol. 28, no. 2, pp. 875–885, Apr. 2013.
[6]R. Gupta, A. Ghosh, and A. Joshi, "Performance comparison of VSC based shunt and series compensators used for load voltage control in distribution systems," IEEE Trans. Power Del., vol. 26, no. 1, pp. 268–278, Jan. 2011.
[7]A. Jain, K. Joshi, A. Behal, and N. Mohan, "Voltage regulation with STATCOMs: modeling, control and results," IEEE Trans. Power Del., vol. 21, no. 2, pp. 726–735, Apr. 2006.
[8]C. Kumar and M. Mishra, "A multifunctional DSTATCOM operating under stiff source," IEEE Trans. Ind. Electron., vol. 61, no. 7, pp. 3131–3136, Jul. 2014.
[9] J. Vasquez, R. Mastromauro, J. Guerrero, and M. Liserre, "Voltage support provided by a droop-controlled multifunctional inverter," IEEE Trans. Ind. Electron., vol. 56, no. 11, pp. 4510–4519, Nov. 2009.
[10] "IEEE recommended practices and requirements for harmonic control in electrical power systems," IEEE Std 519-1992, pp. 1–112, Apr. 1993.
[11]H. Fujita and H. Akagi, "Voltage-regulation performance of a shunt active filter intended for installation on a power distribution system," IEEE Trans. Power Electron., vol. 22, no. 3, pp. 1046–1053, May 2007.
[12]Mahesh K. Mishra, A. Ghosh, and A. Joshi, "Operation of a DSTATCOM in voltage control mode," IEEE Trans. Power Del., vol. 18, no. 1,pp. 258–264, Jan. 2003.

AUTHOR'S PROFILE:

P.Pavaneshwar was born in AP, India in 1993. Currently he is studying his Post graduate degree in Annamacharya Institute of Technology & Sciences, Tirupati affiliated to Jawaharlal Nehru Technological University Anantapur in Electrical and Electronics Engineering with specialization in Electrical Power Systems. His areas of interest include FACTS, Renewable Energy Resources and Power Quality.

Dr.V.C.Veera Reddy is currently working as Professor in Electrical and Electronics Engineering, Annamacharya Institute of Technology & Sciences, Tirupati. He has 36 years of teaching experience. 15 students obtained Ph.D under his guidance. He is also serving as an honorary reviewer for Indian & other reputed journals. He has authored several articles in national and international journals and conferences along with chapters in different books related to Electrical and Electronics Engineering.