ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

Design and Implementation of a Novel Multilevel DC–AC Inverter

[1] L Suresh, [2] R Rajesh
[1] Lecturer, Sree Vidyanikethan Engineering College, Tirupathi
[2] Lecturer, Sree Vidyanikethan Engineering College, Tirupathi

Abstract: **-- In this paper, a novel multilevel dc–ac inverter is pro-posed. The proposed multilevel inverter generates seven-level ac output voltage with the appropriate gate signals' design. Also, the low-pass filter is used to reduce the total harmonic distortion of the sinusoidal output voltage. The switching losses and the voltage stress of power devices can be reduced in the proposed multi-level inverter. The operating principles of the proposed inverter and the voltage balancing method of input capacitors are dis-cussed. Finally, a laboratory prototype multilevel inverter with 400-V input voltage and output 220 Vrms/2 kW is implemented. The multilevel inverter is controlled with sinusoidal pulse-width modulation (SPWM) by TMS320LF2407 digital signal processor (DSP). Experimental results show that the maximum efficiency is 96.9% and the full load efficiency is 94.6%.**

Index Terms—DC–AC inverter, digital signal processor (DSP), maximum power point tracking (MPPT), multilevel.

I. INTRODUCTION

AS A RESULT of high-technology development, the demand and the quality of electric power are higher than before. Because of the advancement of semiconductor, the specification of power device and power conversion technique is promoted. One of the power converters which can trans-form dc–ac is called inverter. Inverter is the intermedium which transmits power to other electrical equipment such as uninter-ruptible power supply, servo motor, air-conditioning system, and smart grid composed of renewable energy shown in Fig. 1. To satisfy different demands and characteristic of loads, the out-put frequency and voltage have to change with different loads .
In recent years, the amount of power equipment is increasing. Therefore, the harmonic pollution of power system becomes more serious. Several standards and regulations have been for-mulated to limit quality of harmonics and power factor of electric equipment such as IEEE Std. 1547 and UL 1741. [4]–[6]. Furthermore, in order to meet the industry requirements for high power applications, the voltage stress of the power device also increases. Although an insulated gate bipolar tran-sistor (IGBT) has features of high power rating and high voltage stress, it cannot operate at high frequency. And the design of IGBT gate driver is complicated. A MOSFET is the appropriate component to operate at high frequency, but power rating is not as good as IGBT. To solve the problem, many different topolo-gies of multilevel use low rating component at high-power application.

The purpose of the multilevel topology is to reduce the volt-age rating of the power switch. Therefore, it usually is used at high-power application. By combining output voltages in mul-tilevel form, it has advantages of low dv/dt, low input current distortion, and lower switching frequency. As a result of advan-tages of multilevel topology, several topologies have emerged in recent years [7], [8].

A novel multilevel inverter is designed and implemented in this paper. The major feature of the proposed topology is the reduction of power components. The sinusoidal pulse-width modulation (SPWM) is used to control proposed circuit by TMS320LF2407 digital signal processor (DSP).

II. POWER STAGE

A. Circuit Configuration

Fig. 2 shows the proposed novel topology used in the seven-level inverter. An input voltage divider is composed of three series capacitors C1, C2, and C3. The divided voltage is trans-mitted to H-bridge by four MOSFETs, and four diodes. The voltage is send to output terminal by H-bridge which is formed by four MOSFETs. The proposed multilevel inverter generates seven-level ac output voltage with the appropriate gate signals design.

B. Operating Principles

The required seven voltage output levels (±1/3Vdc, ±2/3Vdc, ±Vdc, 0) are generated as follows.

1) To generate a voltage level Vo = 1/3Vdc, S1 is turned on at the positive half cycle. Energy is provided by the capac-

IFERP connecting engineers... developing research

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

itor C1 and the voltage across H-bridge is 1/3Vdc. S5 and S8 are turned on, and the voltage applied to the load ter-minals is 1/3Vdc. Fig. 3 shows the current path at this mode.

2) To generate a voltage level Vo = 2/3Vdc, S1 and S4 are turned on. Energy is provided by the capacitor C1 and C2. The voltage across H-bridge is 2/3Vdc. S5 and S8 are turned on, and the voltage applied to the load terminals is 2/3Vdc. Fig. 4 shows the current path at this mode.

3) To generate a voltage level Vo = Vdc, S1 and S2 are turned on. Energy is provided by the capacitor C1, C2, and C3.The voltage across H-bridge is Vdc. S5 and S8 are turned on, and the voltage applied to the load terminals is Vdc. Fig. 5 shows the current path at this mode.

4) To generate a voltage level Vo = −1/3Vdc, S2 is turned on at the negative half cycle. Energy is provided by the capacitor C3, and the voltage across H-bridge is 1/3Vdc. S6 and S7 are turned on, and the voltage applied to the load terminals is −1/3Vdc. Fig. 6 shows the current path at this mode.

5) To generate a voltage level Vo = −2/3Vdc, S2 and S3 are turned on. Energy is provided by the capacitor C2 and C3. The voltage across H-bridge is 2/3Vdc. S6 and S7 are turned on, and the voltage applied to the load terminals is −2/3Vdc. Fig. 7 shows the current path at this mode.

6) To generate a voltage level Vo = −Vdc, S1 and S2 are turned on. Energy is provided by the capacitor C1, C2, and C3, the voltage across H-bridge is Vdc. S6 and S7 is turned on, the voltage applied to the load terminals is −Vdc. Fig. 8 shows the current path at this mode

7) To generate a voltage level Vo = 0, S5 and S7 are turned on. The voltage applied to the load terminals is zero. Fig. 9 shows the current path at this mode.

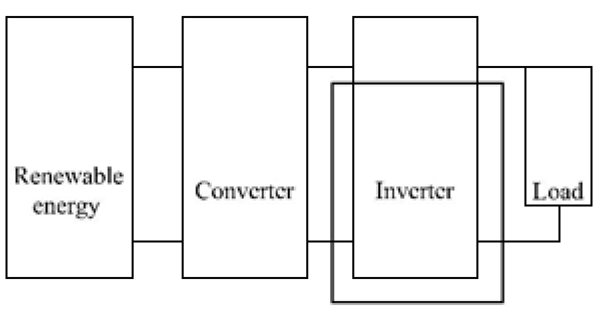


Fig. 1. Block diagram of renewable system.

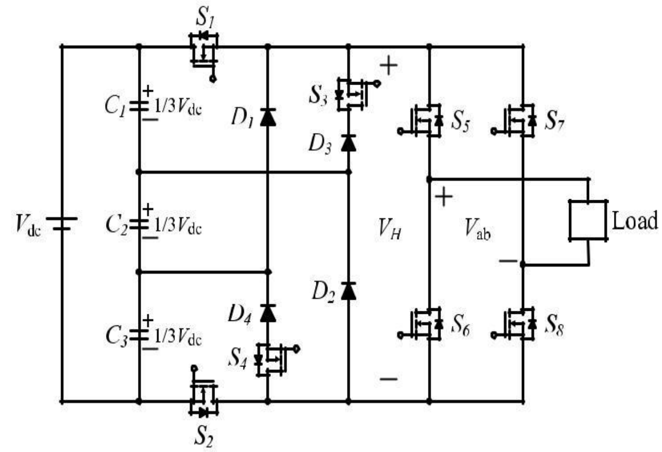
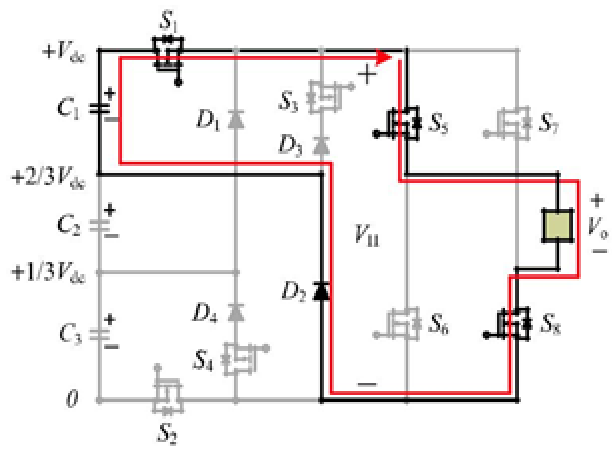


Fig. 2. Proposed seven-level inverter topology



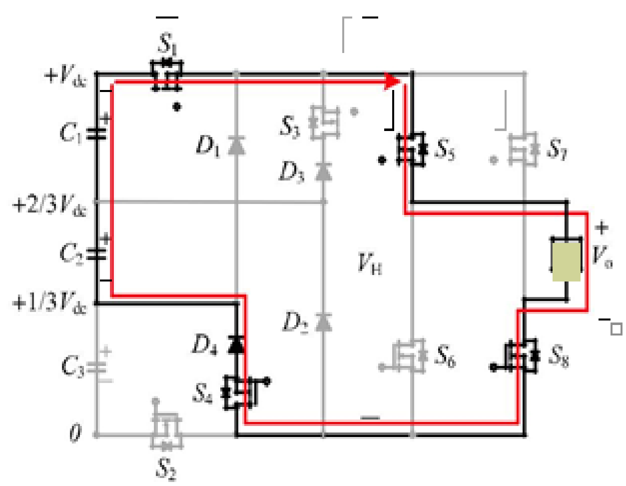


Fig. 3. Switching combination of output voltage level 1/3Vdc.

IFERP
connecting engineers... developing research

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

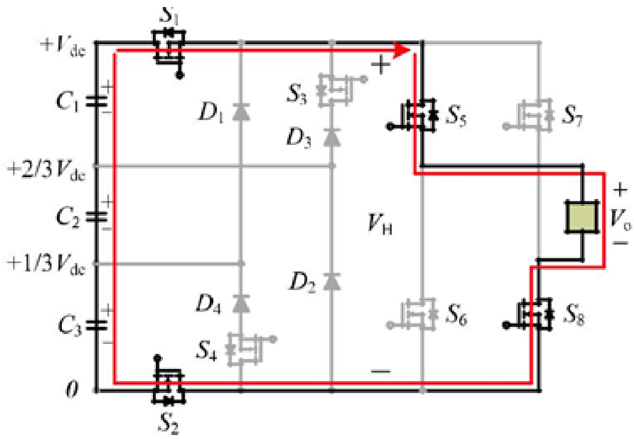


Fig. 4. Switching combination of output voltage level 2/3Vdc

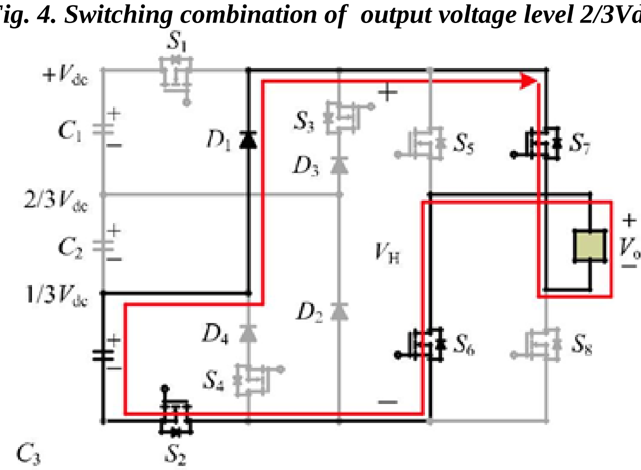


Fig. 6. Switching combination of output voltage level −1/3Vdc

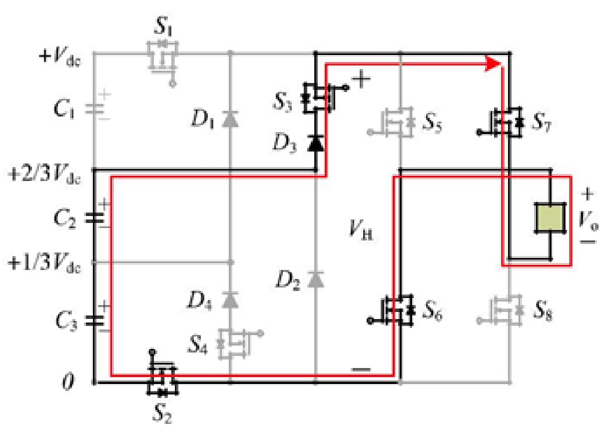


Fig. 7. Switching combination of output voltage level −2/3Vdc

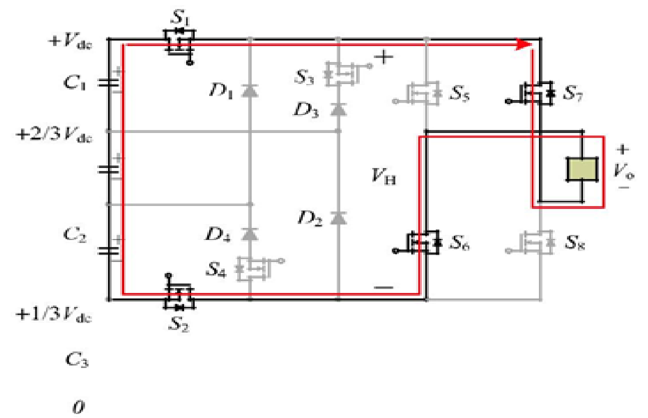


Fig. 8. Switching combination of output voltage level −Vdc.

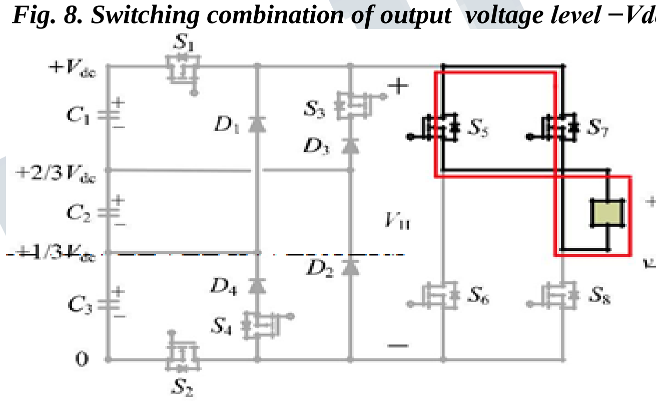


Fig. 9. Switching combination of output voltage level 0.

Table I lists the switching combinations at different output levels.

C. Topology Comparison

TABLE I

Switching Combinations Required To Generate Theseven-Level Output Voltage Waveform

Output voltage V_o	Switching combinations							
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$1/3V_{dc}$	on	off	off	off	on	off	off	on
$2/3V_{dc}$	on	off	off	on	on	off	off	on
V_{dc}	on	on	off	off	on	off	off	on
$-1/3V_{dc}$	off	on	off	off	off	on	on	off
$-2/3V_{dc}$	off	on	on	off	off	on	on	off
$-V_{dc}$	on	on	off	off	off	on	on	off
0	off	off	off	off	on	off	on	off

IFERP connecting engineers... developing research

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

TABLE II
Components comparison between four differentseven-level inverters

	Proposed	Diode-clamped	Capacitor-clamped	Cascaded multicell
Input sources	1	1	1	3
Input capacitors	3	6	2	3
Clamped capacitors	0	0	5	0
Power switches	8	12	12	12
Diodes	4	10	0	0

Table III
Voltage stress comparison between four different

	Proposed	Diode-clamped	Capacitor-clamped	Cascaded multicell
Input sources	V_o	$2V_o$	$2V_o$	$V_o/3$
Input capacitors	$V_o/3$	$V_o/3$	$V_o/2$	$V_o/3$
Power switches	V_o	$V_o/3$	$V_o/3$	$V_o/3$
Diodes	$2V_o/3$	$3V_o/2$	N/A	N/A

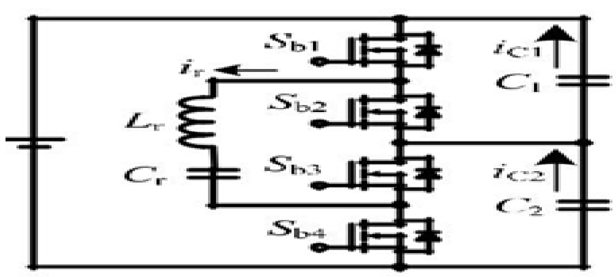


Fig. 10. Circuit configuration of RSCC

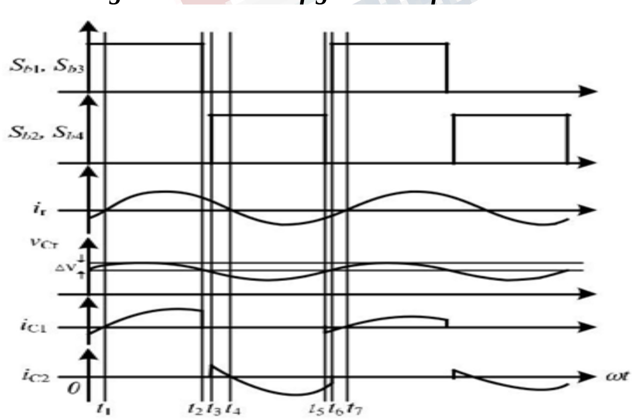


Fig. 11. Waveforms of RSCC

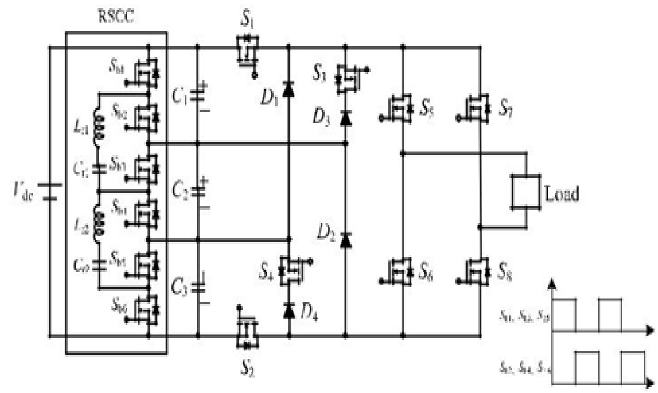


Fig. 12. Proposed multilevel inverter with RSCC

III. VOLTAGE BALANCING CIRCUIT BASED ON RSCC

Since the voltage deviation causes larger harmonics distor-tion in the output voltage, voltage-balancing circuits are indis-pensable for the capacitors in the multilevel inverters [11]–[15]. By

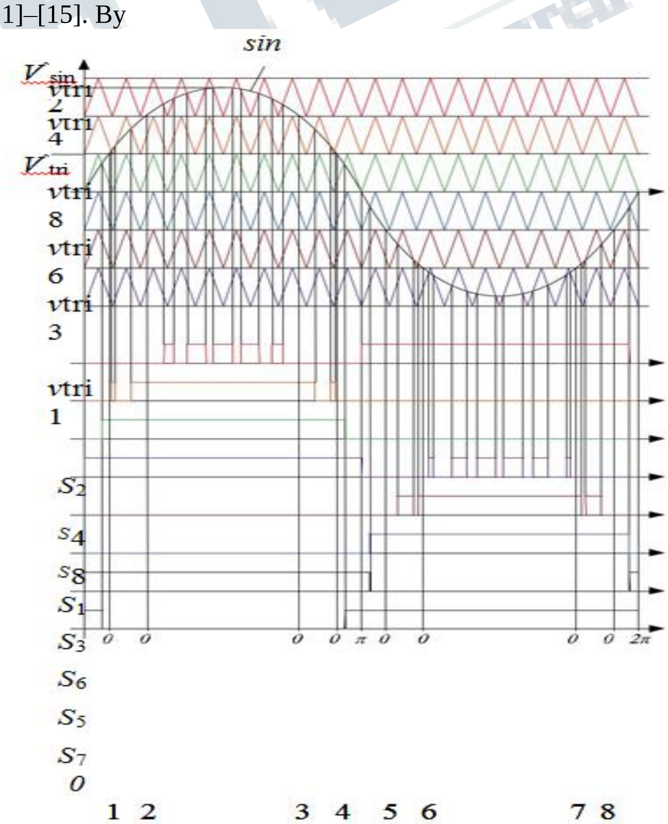


Fig. 13. Reference sine wave, carriers, and control signals of switches

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

using resonant switching capacitor converter, the voltage balance of input capacitors is achieved. Fig. 10 shows the circuit configuration of a unit of the resonant switched-capacitor con-verter (RSCC). The duty cycle of every switch is equal to 50%. The voltage of C1 is higher than the voltage of C2. Since the average current of C1 is higher than that of C2 at one switch-ing cycle, most of the charges flow from C1 to C2. After few switching cycles, the voltages of C1 and C2 are equal. Fig. 11 shows the waveforms of the RSCC.

Fig. 12 shows the configuration of proposed seven-level inverter with RSCC. To apply RSCC at seven-level configu-ration, two switches Sb5 and Sb6, resonant inductor Lr, and resonant capacitor Cr are added. In this application, switches Sb1, Sb3, and Sb5 are turned on at the same time; Sb2, Sb4, and Sb6 are turned on at the same time. The duty of each switch is equal to 50%.

IV. APPLICATION OF SPWM

In this paper, several triangular carriers are distributed by phase disposition technique. The advantage of phase dispo-sition technique is uncomplicated to realize and less total harmonic distortion [16], [17]. These carriers are compared with a reference sine waveform vsin to get signal of switches.
ˆ
The peak-to-peak value of triangular carrier is Vtri. The fre-quency of carrier is switching frequency of inverter. The peak value of reference sine wave is Vsin, and the modulation index mA is defined as

VsinmA = ˆ .   (1)

According to (1), the relationship between the peak value of output sine wave and mA can be expressed as
Vo = mA • Vdc.   (2)

Fig. 13 shows the reference sine wave, carriers, and control signals of switches.

The method that determines switch signals in Fig. 12 is as follows.

1) vsin < 0 and vsin > vtri2 → S2 are turned on

2) vsin > vtri4 → S4 is turned on.
3) vsin < vtri8 → S7 is turned on.
4) vsin > vtri8 → S8 is turned on.

5) vsin > 0 and vsin < vtri1 → S1 are turned on.

6) vsin < vtri3 → S3 is turned on.
7) vsin > vtri6 → S5 is turned on.
8) vsin < vtri6 → S6 is turned on.

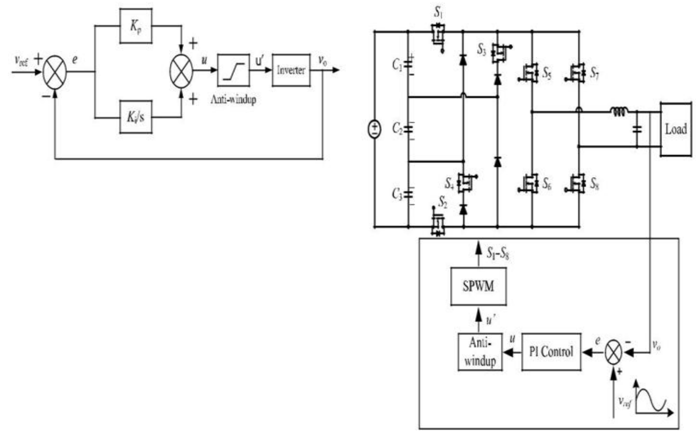


Fig. 14. Block diagram of PI control

V. PI CONTROL USED IN MODIFIED SPWM

Modified SPWM based on PI control is used in this paper [18], [19]. Fig. 14 shows the block diagram of PI control. The block diagram can be expressed in *S* domain as

$$u(s) = \left(K_p + \frac{K_i}{s}\right) e(s). \qquad (3)$$

From (3), the equation can be transformed in the *Z* domain as

$$u(z) = \left(K_p + \frac{K_i}{1 - z^{-1}}\right) e(z). \qquad (4)$$

Then, transform (4) becomes a difference equation is expressed as

$$u[n] = K_p e[n] + K_i e[n] - K_p e[n-1] + u[n-1]. \qquad (5$$

Fig. 15 shows system configuration and control block. System detects output voltage first and compares this signal with a built-in reference. Then, the system feedbacks an error to PI controller. Finally, the PI controller exports a control signal to gate driver.

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

The main idea of modified SPWM is to record the previous error of output voltage and generate a suitable correction at the latest cycle. Because the frequency of carrier is 18 kHz and the frequency of output sine wave is 60 Hz, the number of times of switching is 300 times. Fig. 16 shows the schematic of modified SPWM.

$v_{ref}[n]$ is defined as the reference output voltage, $v_o[n]$ is the feedback of output voltage, and $e[n]$ is error between reference output and feedback output which is expressed as

$$e[n] = v_{ref}[n] - v_o[n]. \qquad (6)$$

Let $K_1 = K_p + K_i$, $K_2 = K_p$, then $e[n]$ is multiplied by K_1 and $e[n - 300]$ multiplied by K_2. Then, add the previous out-put signal $u\ [n - 300]$. Finally, it can obtain the output of PI controller after the process by the anti-windup.

$$u\ [n] = K_1 \cdot e[n] - K_2 \cdot e[n - 300] + u\ [n - 300]. \ (7$$

Fig.15. Seven-level inverter with control algorithm

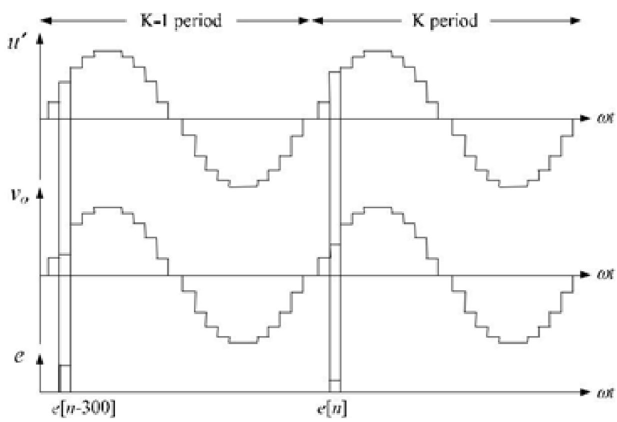


Fig. 16. Schematic of modified SPWM

TABLE IV

Specifications Of The Proposed Inverter

Input voltage V_{dc}	400 V
Output voltage V_o	220 V_{rms}
Rated output power P_o	2 kW
Switching frequency f_s	18 kHz

VI. EXPERIMENT RESULTS

A TMS320LF2407A DSP is used to verify the proposed seven-level inverter. Table IV shows the characteristics of the inverter. Fig. 17 shows the prototype of the seven level inverter. This prototype consists of detect, gate driver, DSP, RSCC, and seven-level inverter.

Fig. 18 presents the output voltage waveform vab showing the desired seven voltage levels and output waveform vo. The seven voltage levels in the figure are ±133, ±267, ±400, and 0 V

Fig. 17. Experimental setup for the prototype

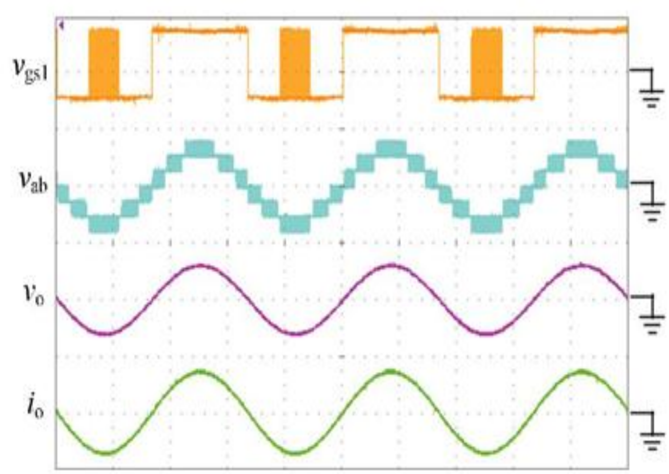


Fig. 18. Waveforms of vgs1, vab, vo, and io at 500 W

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

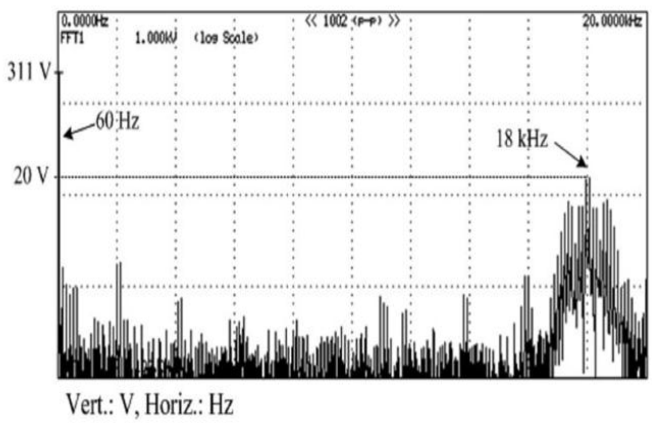


Fig. 19. Output voltage harmonic spectrum of vab calculated by FFT

Figs. 19 and 20 show the output waveform harmonic spectrum calculated by power analyzer YOKOGAWA WT3000 with a proprietary FFT program, and the high-frequency composition is attenuated by LC low-pass filter.

Fig. 21 shows capacitor voltage VC2, output voltage vo, and output current io at 1000 W. In this figure, the capacitor voltage is 133 V. Thus, the function of voltage balancing is achieved. Fig. 22 shows capacitor voltage VC2, output voltage vo, and output current io at 2000 W. The THD of output voltage is 0.9%.

Multilevel structure is usually used in inductive loads such as motor. Thus, this paper applies the proposed topology in induc-tive load. Fig. 23 shows the test block diagram. The inductor and the resistor are connected in series, and PF is set at 0.95.

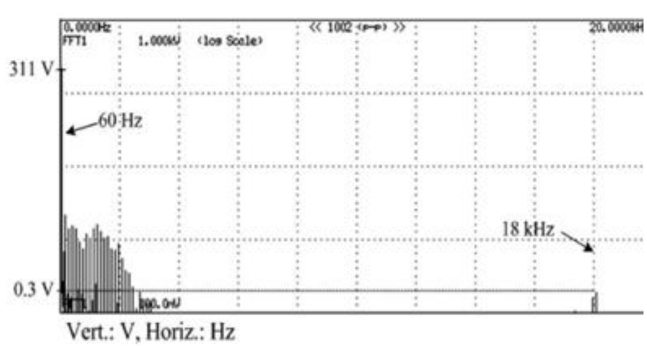


Fig.20.

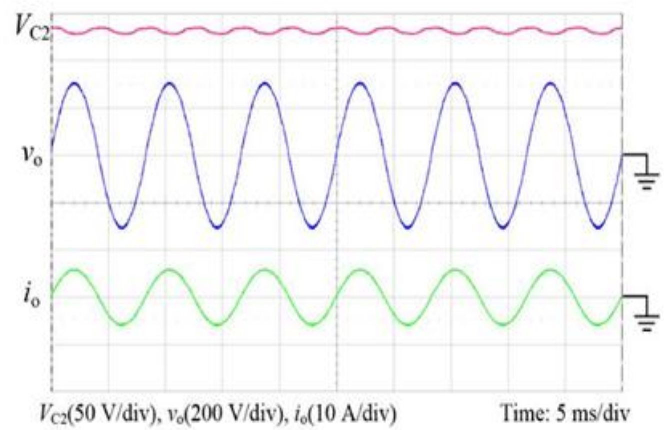


Fig. 21. Waveforms of vC2, vo, and io at 1000 W

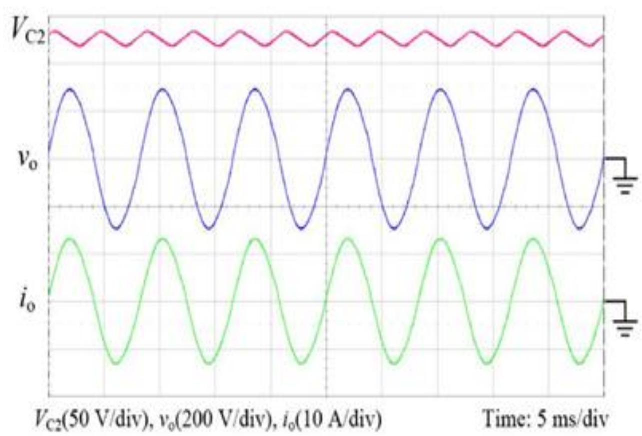


Fig. 22. Waveforms of vC2, vo, and io at 2000 W.

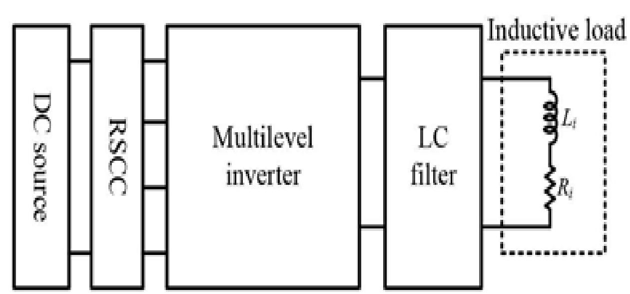


Fig. 23. Test block diagram of inductive load Fig. 24 shows the output voltage and current at 400 VA. The THD of output voltage is 3.3%. The efficiency at different output power is shown in Fig. 25. The output power is from 200 W to 2000 W. The highest effi-ciency is 96.9% at 800 W, and the lowest is 94.6% at 2000 W. The efficiency is always above 94.5%.

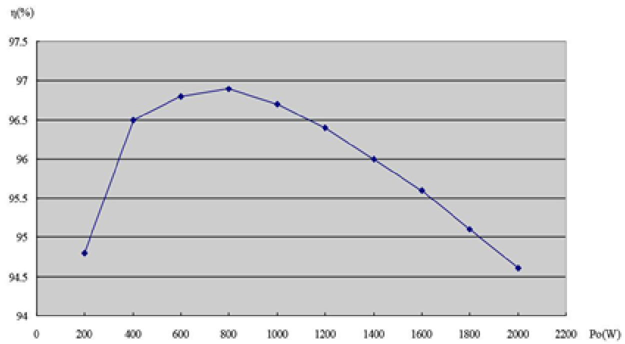


Fig. 25. Efficiency of the proposed inverter

VII. CONCLUSION

A novel seven-level inverter was designed and implemented with DSP in this paper. The main idea of the proposed configuration is to reduce the number of power device. The reduction of power device is proved by comparing with traditional structures. Finally, a laboratory prototype of seven-level inverter with 400-V input voltage and output 220 Vrms/2 kW is implemented. Experimental results show that the maximum efficiency is 96.9% and the full load efficiency is 94.6%.

REFERENCES

[1] R. Gonzalez, E. Gubia, J. Lopez, and L. Marroyo, "Transformerless single-phase multilevel-based photovoltaic inverter," IEEE Trans. Ind. Electron., vol. 55, no. 7, pp. 2694–2702, Jul. 2008.

[2] S. Daher, J. Schmid, and F. L. M. Antunes, "Multilevel inverter topologies for stand-alone PV systems," IEEE Trans. Ind. Electron., vol. 55, no. 7, pp. 2703–2712, Jul. 2008.

[3] W. Yu, J. S. Lai, H. Qian, and C. Hutchens, "High-efficiency MOSFET inverter with H6-type configuration for photovoltaic nonisolated, ac-module applications," IEEE Trans. Power Electron., vol. 26, no. 4, pp. 1253–1260, Apr. 2011.

[4] R. A. Ahmed, S. Mekhilef, and W. P. Hew, "New multilevel inverter topology with minimum number of switches," in Proc. IEEE Region 10 Conf. (TENCON), 2010, pp. 1862–1867.

[5] M. R. Banaei and E. Salary, "New multilevel inverter with reduction of switches and gate driver," in Proc. IEEE 18th Iran. Conf. Elect. Eng. (IECC), 2010, pp. 784–789.

[6] N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven-level grid-connected inverter for photovoltaic system," IEEE Trans. Ind. Electron., vol. 58, no. 6, pp. 2435–2443, Jun. 2011.

[7] K. Hasegawa and H. Akagi, "A new dc-voltage-balancing circuit includ-ing a single coupled inductor for a five-level diode-clamped PWM inverter," IEEE Trans. Ind. Appl., vol. 47, no. 2, pp. 841–852, Mar./Apr. 2011.

[8] T. Ito, M. Kamaga, Y. Sato, and H. Ohashi, "An investigation of voltage balancing circuit for dc capacitors in diode-clamped multilevel inverters to realize high output power density converters," in Proc. IEEE Energy Convers. Congr. Expo. (ECCE), 2010, pp. 3675–3682.

[9] A. Shukla, A. Ghosh, and A. Joshi, "Flying-capacitor-based chopper circuit for dc capacitor voltage balancing in diode-clamped multilevel inverter," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2249–2261, Jul. 2010.

[10] C. L. Xia, X. Gu, T. N. Shi, and Y. Yan, "Neutral-point potential balancing of three-level inverters in direct-driven wind energy conversion system," IEEE Trans. Energy Convers., vol. 26, no. 1, pp. 18–29, Mar. 2011.

[11] K. Sano and H. Fujita, "Voltage-balancing circuit based on a resonant switched-capacitor converter for multilevel inverters," IEEE Trans. Ind. Appl., vol. 44, no. 6, pp. 1768–1776, Nov./Dec. 2008.

[12] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral point clamped inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[13] Suroso and T. Noguchi, "New generalized multilevel current-source PWM inverter with no-isolated switching devices," in Proc. IEEE Int. Conf. Power Electron. Drive Syst. (PEDS), 2009, pp. 314–319.

[14] J. Selvaraj and N. A. Rahim, "Multilevel inverter for grid-connected PV system employing digital PI controller," IEEE Trans. Ind. Electron., vol. 56, no. 1, pp. 149–158, Jan. 2009.

[15] N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven-level grid-connected inverter for photovoltaic system," IEEE Trans. Ind. Electron., vol. 58, no. 6, pp. 2435–2443, Jun. 2011.

[16] N. Vazquez, H. Lopez, C. Hernandez, E. Vazquez, R. Osorio, and J. Arau, "A different multilevel current-source inverter," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2623–2632, Aug. 2010.

[17] K. A. Tehrani, I. Rasoanarivo, H. Andriatsioharana, and F. M. Sargos, "A new multilevel inverter model NP without clamping diodes," in Proc. 34th Annu. Conf. IEEE Ind. Electron. Soc. (IECON), 2008, pp. 466–472.

[18] G. Ceglia et al., "A new multilevel inverter topology," in Proc. Devices Circuits Syst., 2004, vol. 1, pp. 212–218.

[19] D. A. B. Zambra, C. Rech, and J. R. Pinheiro, "Comparison of neutral-point-clamped, symmetrical, and hybrid asymmetrical multilevel invert-ers," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2297–2306, Jul. 2010.

AUTHOR:

He completed M.Tech in 2013 from SVPCET, Puttur. He has a teaching experience of 8 years .Present he is working as a Lecturer in Sree Vidyanikethan Engineering College.Tirupathi. His areas of interest power electronics and control systems

