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A Power Quality Improved Bridgeless Converter with fuzzy logic controller Based Computer Power Supply

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***Abstract*: -- Poor power quality, moderate dynamic reaction, high gadget stretch, consonant rich, occasionally thick, peaky, mutilated info current are the significant issues which are every now and again experienced in traditional switched mode power supplies (SMPSs) utilized as a part of personal computers (PCs). To overcome these issues, it is proposed here to utilize a non-isolated bridgeless buck-support single ended primary inductance converter (SEPIC) in discontinuous conduction mode (DCM) at the front end of a SMPS. The bridgeless SEPIC at the front end gives solidly controlled output dc voltage even under successive information voltage and load varieties. The output of the front-end converter is connected with a half scaffold dc-dc converter for seclusion and furthermore to obtain distinctive dc voltage levels at the heap end that are required in a PC. Controlling a solitary output voltage can direct the various dc output voltages also**

Keywords— Bridgeless converter; PFC; input current; computer power supply; power quality.

I. INTRODUCTION

Many electronic apparatuses controlled up from the utility, use the established strategy for ac dc amendment which includes a diode bridge rectifier(DBR) trailed by a huge electrolytic capacitor. The uncontrolled charging and releasing of this capacitor actuates consonant rich current being drawn from the utility which conflicts with the universal influence quality standard cutoff points [1-2]. Present day ac-dc converters consolidate power factor correction(PFC) and consonant current decrease at the purpose of regular coupling (PCC) which enhances voltage direction and productivity [3-5] at the load end. (PC) is one of the electronic gear which is seriously influenced by power quality issues. Single stage and two-phase transformations of ac voltage into dc voltage have been utilized as a part of PCs to keep up consonant substance inside cutoff points and furthermore to get solidly managed various outputs. Single stage power transformation is basic, smaller and savvy. Be that as it may, it experiences poor dynamic reaction, control multifaceted nature, high capacitance esteem and high segment push. In this way, two phase change of ac voltage into different dc voltages is for the most part favored in PCs [6]. The segment tally in a two-phase control supply is significantly higher than its single stage partner. In any case, it gives better output voltage direction, quick unique reaction and hinders the second symphonious (100Hz or 120Hz) segment in the main stage itself so that huge capacitors at the output side are avoided.

Different front end converters have been utilized in the power supplies for giving PFC and output voltage control. A lift converter is the basic decision for giving PFC in power supplies. Nonetheless, it is not the favored decision in PC control supplies because of its necessity for an expansive info voltage run [7]. The output voltage of a lift converter can't be controlled to an esteem under 300V for a 220V ac input. Along these lines, a buck-support converter is favored in PCs where wide varieties in input voltages and load are normal [8-9]. Low output voltage swell is favored in a PC control supply as it is connected with different ICs. Single stage power supplies are utilized as a part of numerous applications where control quality change and voltage direction happen in a solitary stage. Be that as it may, in PCs, single stage setup builds the worry over the switches and moderates the voltage direction under changing burdens. Consequently, two phase PFC ac dc converters based SMPSs are being utilized to enhance the information control quality and furthermore to get an adequate output voltage direction. Be that as it may, the productivity of a two phase SMPS is lower than the ordinary SMPS. To wipe out this burden, another bridgeless front-end converter is proposed in this paper for PC control supplies which offers low exchanging swell, sinusoidal information present and great dynamic reaction when contrasted with other non-disconnected buck-help converters. The end of DBR at the front final products in decreased

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conduction misfortunes and backings a bigger output voltage run with upgraded proficiency. At the output of the front-end converter, a half scaffold converter is utilized which gives detachment, control and different dc outputs [18-20] with a superior center usage.

It is seen from the accessible writing that the power quality change in SMPSs utilizing bridgeless PFC converter has not been endeavored by numerous specialists up until this point. In this work, a bridgeless single finished essential inductance converter (SEPIC) working in broken conduction mode (DCM) is being utilized at the front end of the SMPS which offers magnificent PFC at the appraised and in addition light load condition. Upper converter works in the positive half cycle of the air conditioner voltage while the lower converter works in the negative half cycle. The output of the bridgeless PFC converter is connected with the detached converter. Test consequences of the proposed different output SMPS are found in accordance with the mimicked execution exhibiting its enhanced power quality and output voltage control.

II. SMPS CONFIGURATION AND OPERATING PRINCIPLE

The proposed PC control supply comprises of chiefly two sections, bridgeless front-end ac-dc converter and multi-output disconnected dc-dc converter. The working mode out of CCM (Continuous Conduction Mode) or DCM of the bridgeless front-end converter might be chosen on the necessity of the client. A DCM is chosen if the cost is a noteworthy thought; if not, CCM is received that lessens gadget worries, regardless of the way that two voltages and one current sensor are required which makes it costlier. Consequently, a DCM operation of the front-end PFC converter is favored in PCs where just a single voltage sensor is required for detecting furthermore, control. Here, the front-end converter is outlined in DCM for accomplishing inalienable PFC which requires just a single voltage sensor while the disengaged converter is composed in CCM.

The control circles of both converters are free of each other. The system design and working rule of SMPS system has been depicted in taking after subsections.

A. System Configuration

The design of proposed power supply with four directed dc output voltages is appeared in Fig.1. At the info side, DBR is disposed of by utilizing two SEPICs. The upper converter works in the positive half cycle and the lower one work in the negative half cycle of the information ac voltage. The exchanging frequency of both the converters is set at 20 kHz for effective control. The outline of output inductors for both the converters is completed in DCM to decrease the intricacy in control. The control of the output voltage can take care of wide varieties in the information voltage and the heap. The output dc voltage (V_{PFC}) is detected and contrasted and a reference voltage ((V_{PFCref}) from which the voltage mistake is acquired ($V_{Epfc}=V_{PFCref}-V_{PFC}$) which is given to a corresponding furthermore, basic (PI) controller. The PI controller output (Vcc1) is contrasted and a high frequency saw-tooth 1 wave to output PWM beats that are given to both switches all the while. In the event that St<Vcc1 and V_{ac} is certain, at that point Sp is on, else Sp stays off. St speaks to the exchanging signals for the bridgeless ac-dc converter. The width of these PWM beats shifts as indicated by the output of the PI voltage controller-1 so that the output dc voltage VPFC is directed adequately which is, thusly, nourished to the disconnected half extension converter in the second stage to acquire different secluded directed output voltages. Thus, the width of PWM heartbeats changes as needs be to keep up dc output voltage VPFC steady. The seclusion is affected through multi winding high frequency transformer (HFT). An inside tapped arrangement is picked at the yield side to decrease the conduction misfortunes. All the optional windings are controlled through one control circle. The most elevated appraised optional twisting of the HFT is chosen for voltage detecting. The distinction between the yield voltage (Vo1) and reference voltage (Vo1ref) is encouraged to another PI voltage controller-2 which yield is contrasted and another high frequency saw-tooth wave 2 to create second arrangement of PWM signs for the half-connect converter gadgets S1 and S2. Care ought to be taken to make beyond any doubt that there is adequate dead-time between killing of S1 and turn-on of S2 to maintain a strategic distance from shoot-through blame. The confined converter is worked in CCM to take the upside of decreased stretch. In the event that the heap in any of the winding changes, the obligation cycle changes in like manner to guarantee managed dc voltage yields. The reaction of alternate yields is slower than the one where the yield voltage is detected.

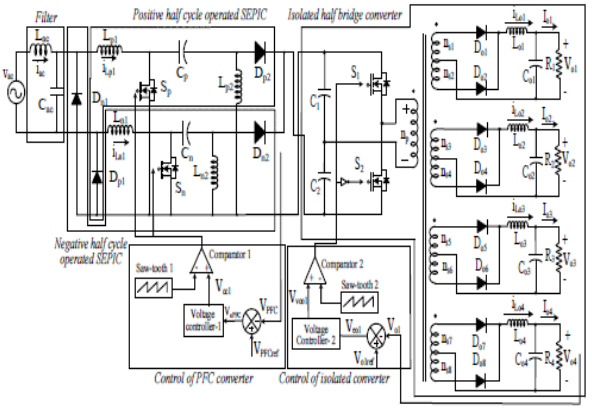

Fig.1 Schematic diagram of the PFC converter based SMPS

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B. Operating Principle

The operation of the front-end converters and the isolated converter are described independently as follows:

1) Operating principle of front end converter

Amid the positive half cycle of the information voltage, the upper SEPIC works as appeared in Fig. 2. Similarly, amid negative half cycle the lower SEPIC would work. The operation of the SEPIC in one PWM cycle is portrayed with the assistance of the accompanying modes: In the primary mode, the high frequency switch Sp turns on, the information inductor Lp1 begins putting away the vitality which is exchanged from the single stage ac mains as appeared in Fig. 3a. Diode Dp1 finishes the present way. In the second mode, Sp is killed and diode Dp2 begins directing. The vitality in yield inductor Lp2 begins diminishing to zero which is appeared in Fig. 3b. In the last exchanging state, the current in the yield inductor stays zero until the begin of next exchanging cycle. This mode guarantees the DCM operation as appeared in Fig. 3c.

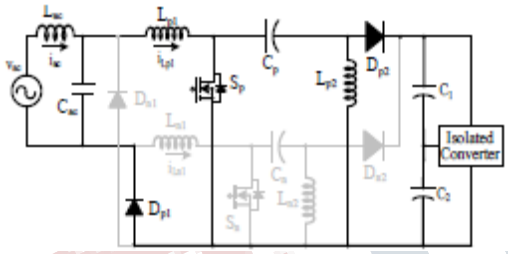

Fig. 2 Operation of PFC converter when the input voltage is positive

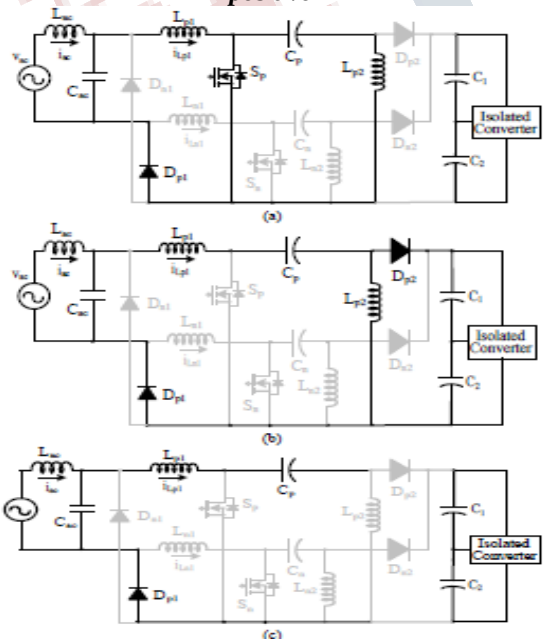

Fig. 3 Operating modes of bridgeless PFC converter when the input voltage is positive

2) Operating principle of isolated converter

Two high frequency switches are turned on and off on the other hand in one exchanging cycle. In this way, the operation of the converter in one portion of the exchanging cycle is the same as that of the other half cycle. In the primary half cycle, the upper switch S1 is turned on. The diodes on the auxiliary side (Do1, Do3, Do5 and Do7) begin directing and the inductors (Lo1-Lo4) in all the optional windings begin putting away vitality. At the point when the inductor current achieves its most extreme esteem, upper turn S1 is killed. All the channel capacitors release through the heaps to keep up dc yield voltages as consistent. In the following half cycle of the PWM period, the upper turn is killed. The auxiliary diodes (Do1-Do8) are swung on to free-wheel the inductors streams. The current in every single auxiliary winding scratch off center flux so that net voltage crosswise over HFT ends up noticeably zero. A similar inductor charging and releasing happen in next half exchanging cycle with the lower switch S2.

III. DESIGN OF PROPOSED BRIDGELESS CONVERTER BASED SMPS SYSTEM

The design of proposed bridgeless converter based SMPS is described in the following section.

A. Design of Proposed SMPS System

The design for the positive half cycle operated PFC converter is carried out here. The negative half cycle operated converter is designed in the same way. The average voltage Vacav is calculated as,

$$V_{acav} = \frac{2\sqrt{2V_{ac}} \times 220V}{\pi} = 198\,V \qquad (1)$$

The duty cycle D of the PFC buck-boost converter is expressed as the ratio of its output dc voltage to the sum of output dc voltage and input voltage.

$$D = \frac{V_{PFC}}{V_{PFC} + V_{acvc}} = \frac{300V}{300V + 198V} = 0.6 \qquad (2)$$

Irrespective of variation in the input voltage from 170V to 270V, the output voltage is maintained constant at 300V. Hence, the duty cycles for supply voltages of 170V voltage, 220V and 270V are calculated as, D170V=0.66, D220V=0.6, D270V=0.552 respectively. The duty cycle D of the PFC converter is taken less than D220V for an efficient control during DCM operation. Therefore, it is considered as 0.25 for the design of the PFC converter.

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The input inductor value is calculated for the permitted ripple of 40% of input current

$$L_{P1} = \frac{DV_{acavg}}{f \times (i_{inripple})} = \frac{0.25 \times 198V}{20kHz \times 0.58A} = 4.35\ mH \quad (3)$$

Where, f is the switching frequency of the PFC converter. The critical conduction parameter is given as,

$$K_a < \frac{1}{2\left(\frac{V_{PFC}}{\sqrt{2}V_{ac}}+n\right)^2} = \frac{1}{2\left(\frac{300V}{311V}+1\right)^2} = 0.129 \quad (4)$$

Where, n is taken as 1 for the non-isolated PFC converter. To operate the PFC converter in DCM, the conduction parameter should be taken less than Ka for efficient control. Hence, it is selected as 0.08.

The equivalent value of inductance of the PFC converter is given as,

$$L_{eq} = \frac{R_{dc}K_a}{2f} = \frac{281.2\Omega \times 0.08}{2 \times 20kHz} = 225\ \mu F \quad (5)$$

Therefore, the output inductor value is calculated as,

$$L_{P2} = \frac{L_{P1}L_{eq}}{L_{P1}-L_{eq}} = \frac{4.31mH \times 225\mu H}{4.31mH-225\mu H} = 237\ \mu H \quad (6)$$

The selected value of output inductor is 100 µH to ensure DCM condition in all operating conditions of input voltages, load and unity PF operation at a low input voltage.

The intermediate capacitor value is estimated as,

$$C_P = \frac{1}{\omega_{P(L_{P1}+L_{P2})}} = \frac{1}{2 \times \pi \times 2000Hz \times (4.3mH+0.1mH)} = 0.18\mu F \quad (7)$$

where, ωr is the angular frequency (ωr=2πfr). A fr is considered as 2000Hz (f>fr>fL). A capacitor value of 0.22µF is selected for the hardware implementation.

An L-C filter is used at the input side to mitigate higher order harmonics [22]. The maximum value of the capacitor is as,

$$C_{ac} = \frac{I_P tan\theta}{\omega V} = \frac{2.25A \times 0.017}{314 \times 311V} = 391\ nF \quad (8)$$

The filter capacitor value is selected such that it is less than Cac. Hence, a 330nF capacitor is selected in hardware implementation.

The filter inductor Lac is calculated for mitigating high order harmonics close to 5 kHz frequency.

$$L_{ac} = \frac{1}{4\pi^2 f_c^2 C_d} = \frac{1}{4 \times (3.14 \times 5 \times 10)^2 \times 330 \times 10^{-9}} = 3.07\ mH \quad (9)$$

A 3.1mH inductor is selected for simulation and experimental system.

The input capacitors of the isolated half bridge dc-dc converter act as the output filter capacitors for the PFC converter. So, the design of the capacitor is important to eliminate the second order harmonic component as well as to provide maximum power for that duration when input voltage falls. This is very crucial for PC power supplies as the rating of the capacitor affects the size and the cost of the overall SMPS.

The expression for calculating the capacitor to reduce second order harmonic is as [3],

$$\frac{C_1}{2} = \frac{C_2}{2} = \frac{I_{PFC}}{2\omega\Delta V_{PFC}} = \frac{1.06A}{2 \times 314 \times 6V} = 0.28\ mF \quad (10)$$

The hold-up capability can be estimated as,

$$t_{hold-up} = \left({V_{PFC_m}}^2 - {V_{PFC_{min}}}^2\right)\frac{C}{2P_0} \quad (11)$$

where, thold-up is the holdup time of the capacitor, Po is the maximum output power, V_{PFC} m is the minimum output voltage (2% ripple is considered) and V_{PFC} min is the minimum voltage at which the output voltage holds regulation.

Therefore, to maintain 10ms hold-up time, the required capacitance is calculated as,

$$\frac{2t_{hold-up}P_0}{\left({V_{PFC_m}}^2 - {V_{PFC_{min}}}^2\right)} = \frac{2 \times 10 \times 30W}{(294V)^2-(260V)^2} = 0.339\ mF \quad (12)$$

Two capacitors are connected in series. Therefore, the value of C1=C2=0.679 mF. The selected value of the capacitors is 0.6mF each to meet both the conditions.

The calculation of inductance for the secondary winding with highest rating is shown here, while the calculation for rest of the secondary windings remains same. The inductance Lo1 is expressed as,

$$L_{01} = \frac{V_{01}(0.5-D_s)}{f_s \Delta i_{Lo1}} = \frac{12V(0.5-0.4)}{60kHz \times 0.624A} = 0.032mH \quad (13)$$

Similarly, the inductances for the other secondary windings are calculated as 9.5 µH, 6.8 µH and 1.5 mH.

IV. FUZZY CONTROLLER

Fuzzy logic is a complex mathematical method allows to lower complexity by allowing the use of imperfect information in sensible way. It can be implemented in hardware, software, or a combination of both. In other words, fuzzy logic approach to problems' control mimics how a person would make decisions, only much faster**.** The PI controller requires precise linear mathematical models, which are difficult to obtain and may not give satisfactory performance under parameter variations, load disturbances, etc. Recently, Fuzzy Logic Controllers (FLCs) have been introduced in various applications and have been

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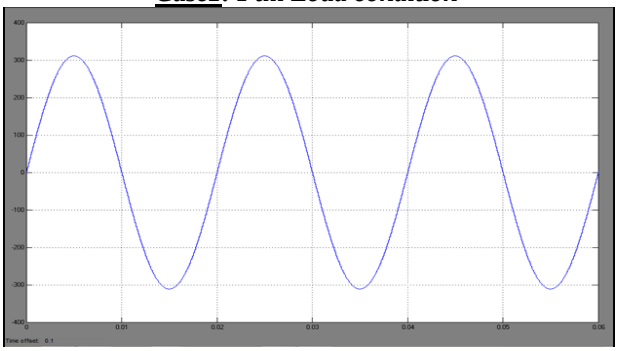
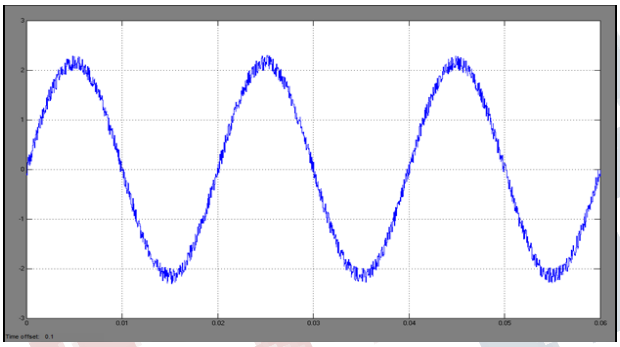
used in the power electronics field. The advantages of fuzzy logic controllers over conventional PI controllers are that they do not need an accurate mathematical model, Can work with imprecise inputs and Can handle non-linearities and are more robust than conventional PI controllers.

Case1: Full Load condition



Vac



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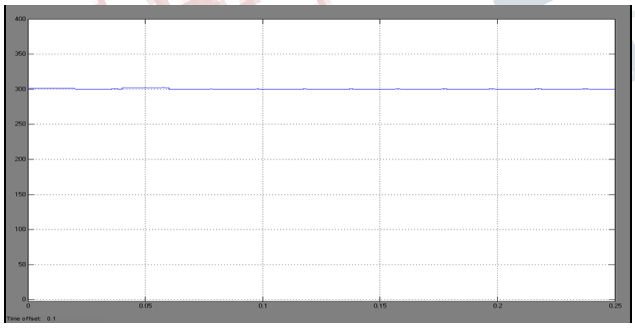
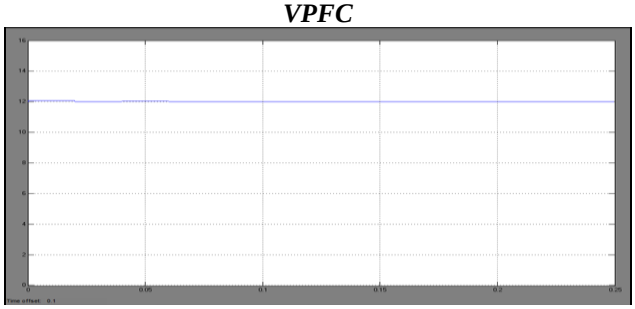
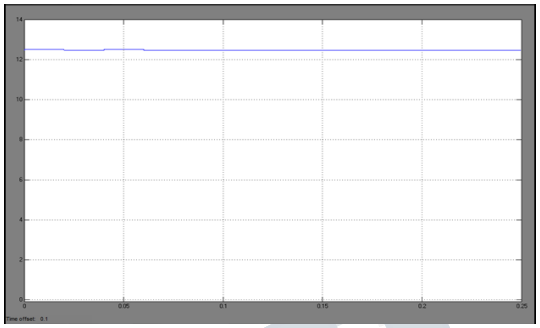


VPFC



V01



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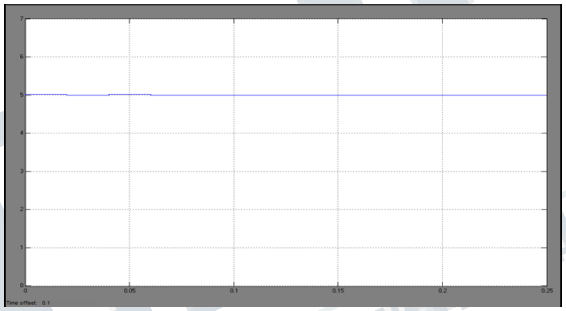
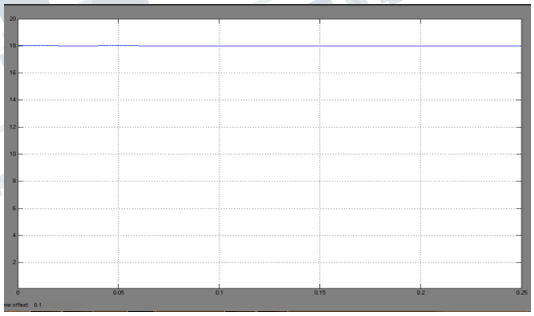


V02



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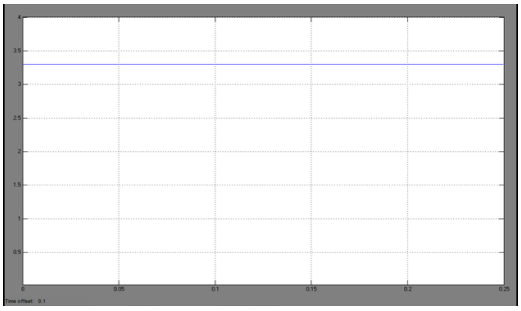

V03

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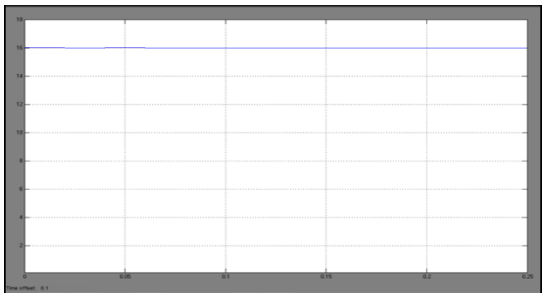

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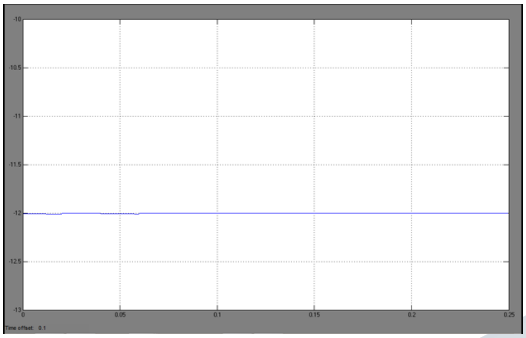

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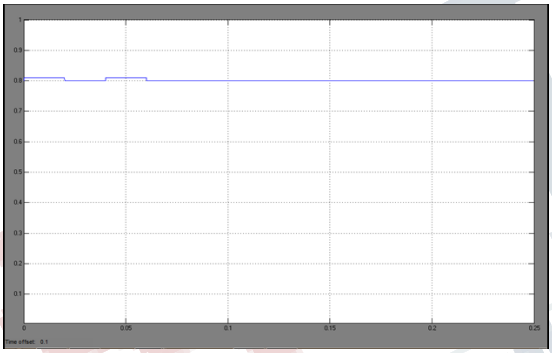

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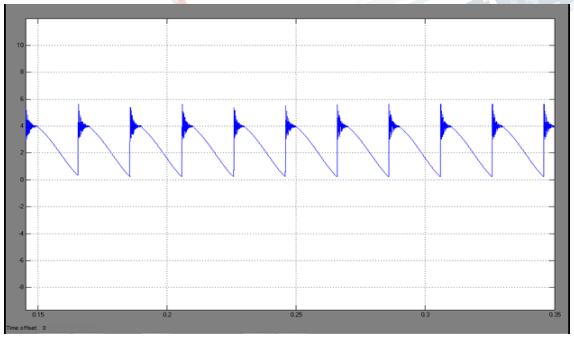
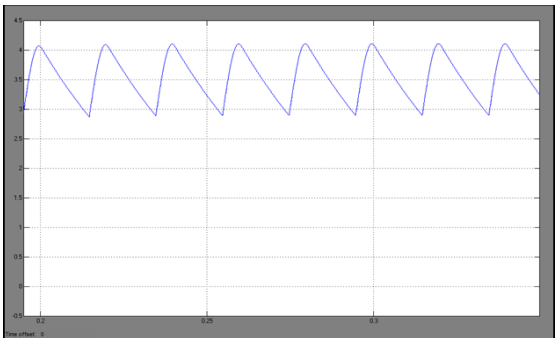


ILP1



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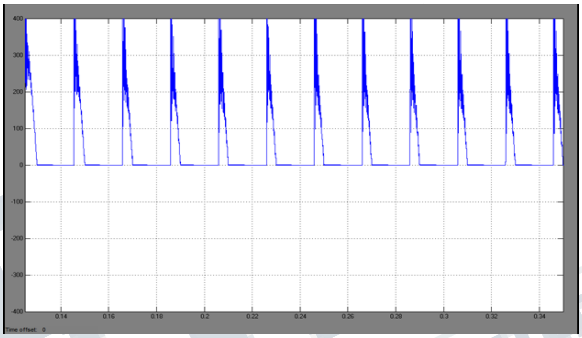
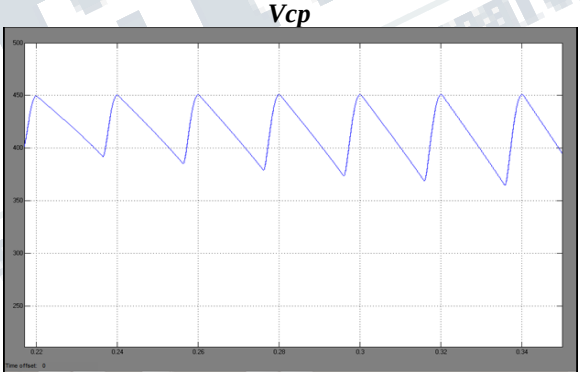
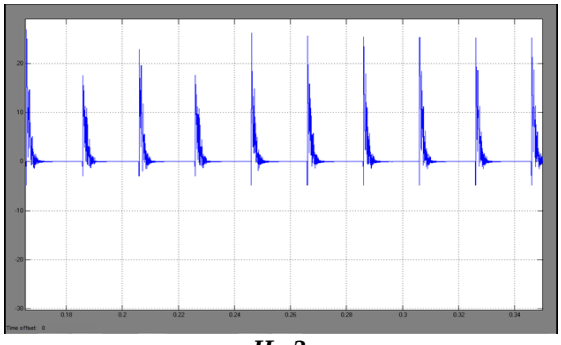


Vcp



Vcn



ILp2

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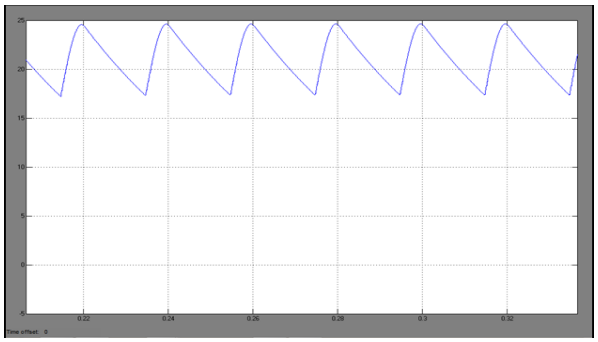

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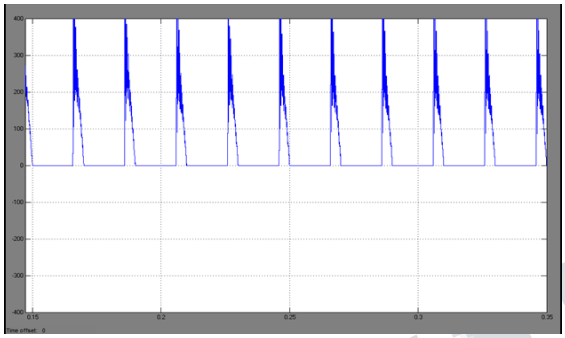

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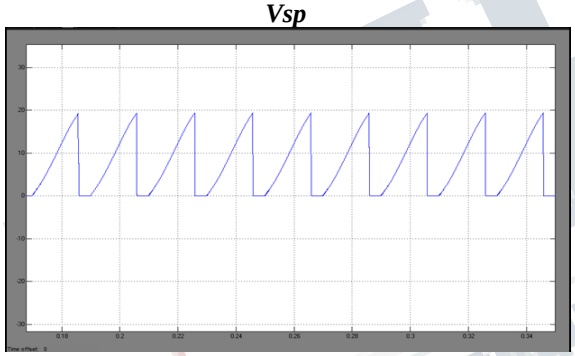
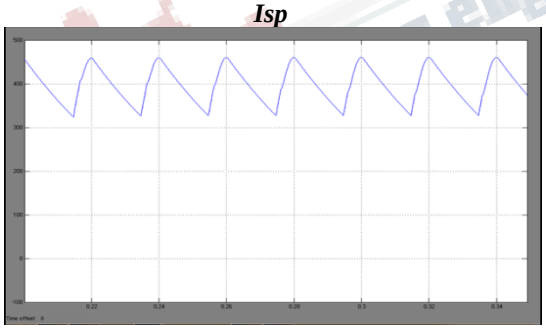


Isp



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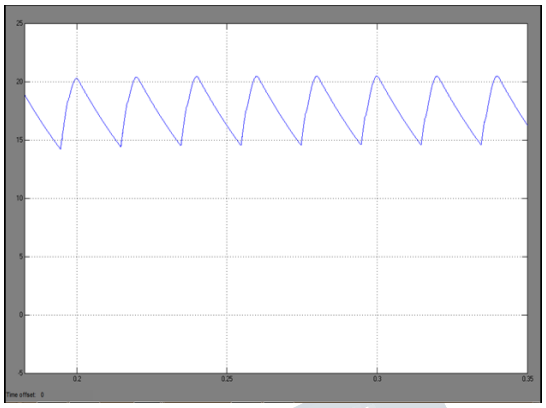

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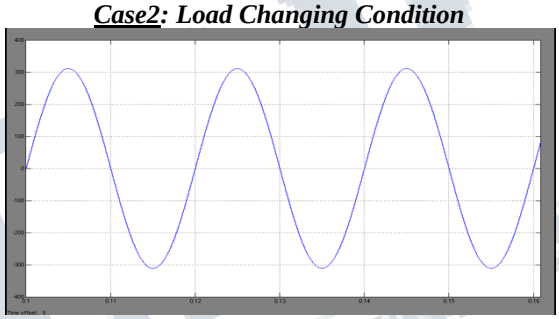
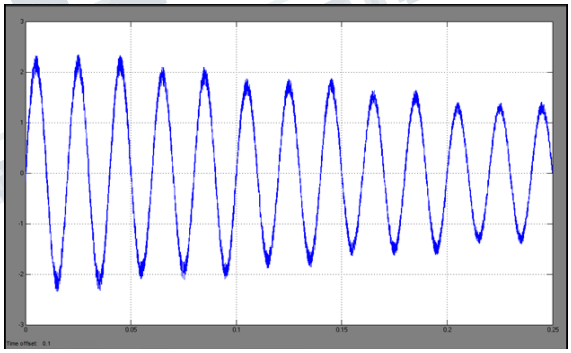
***Case2*: Load Changing Condition**



Vac



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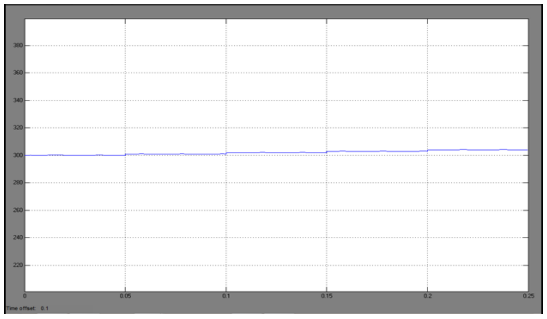

Vpfc

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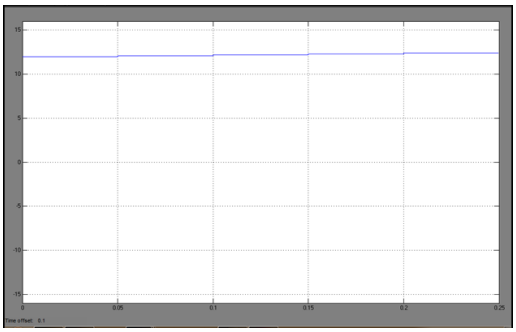

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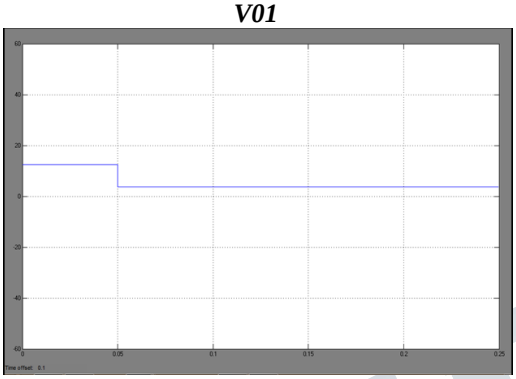

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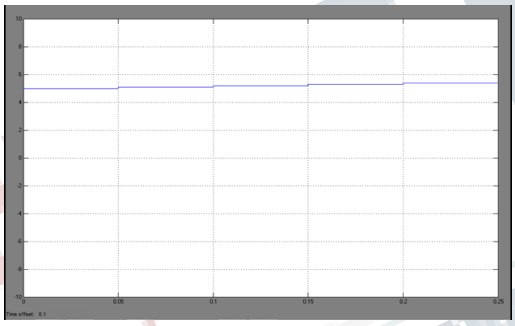

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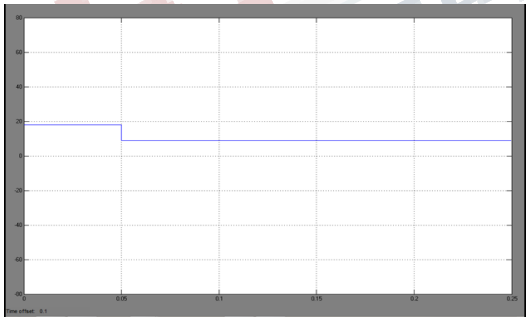

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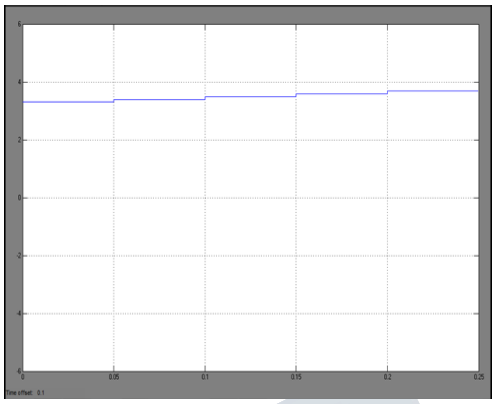

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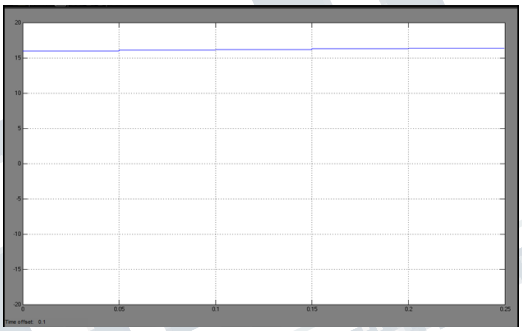

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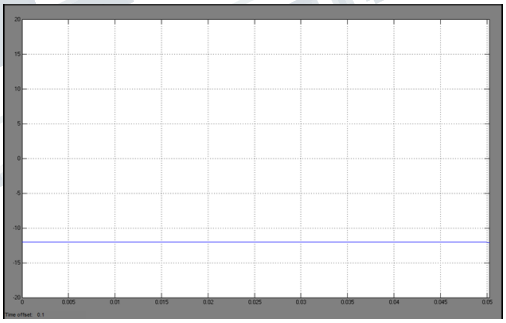

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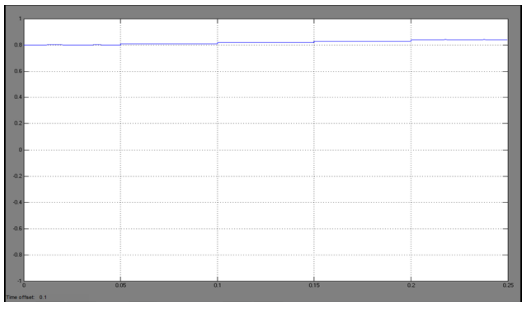

I04

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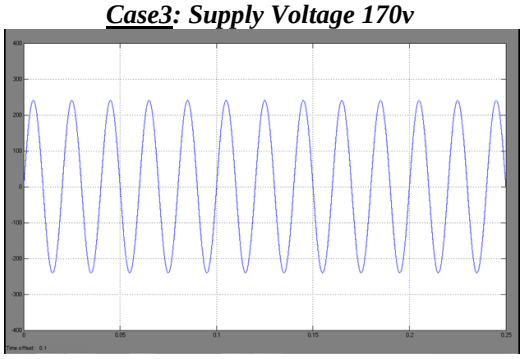
Case3: Supply Voltage 170v



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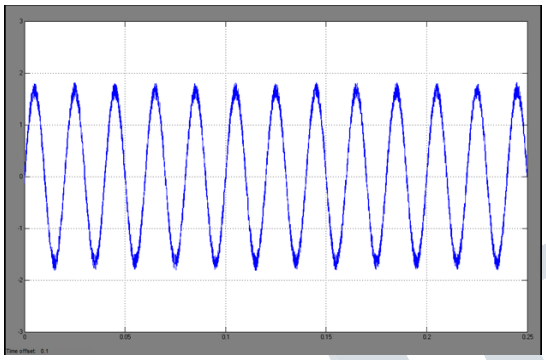

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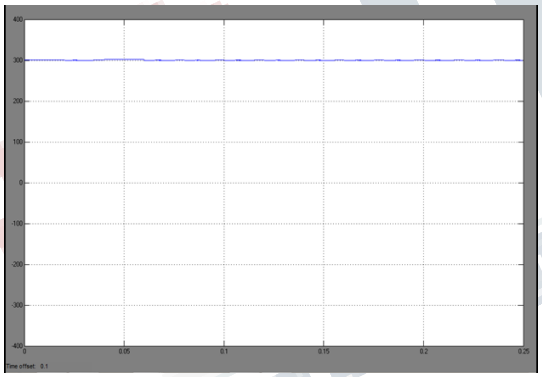

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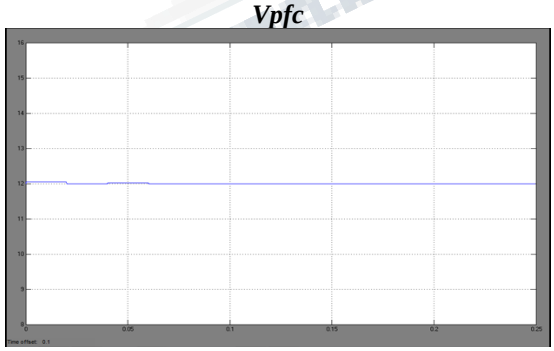

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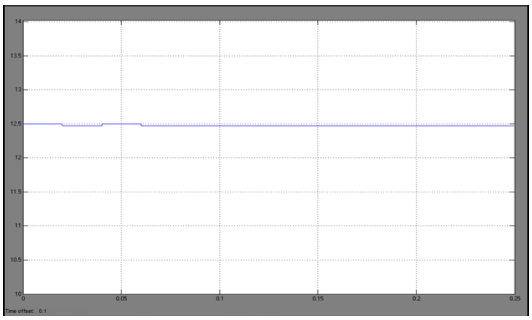

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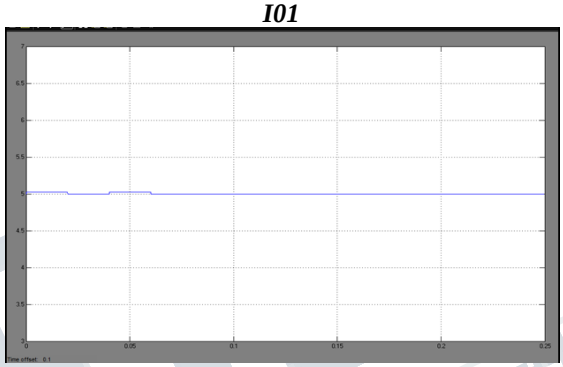

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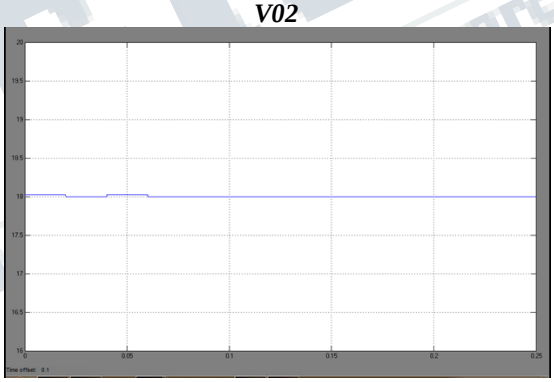

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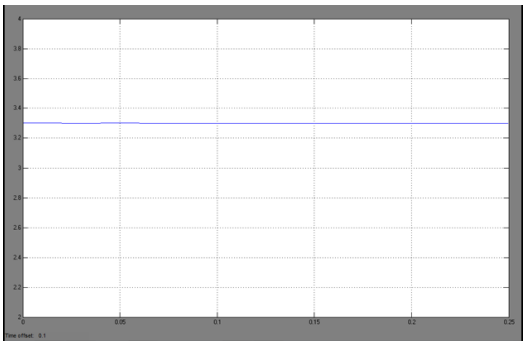

V03

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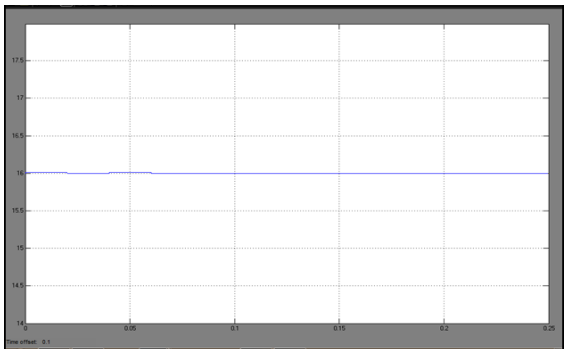

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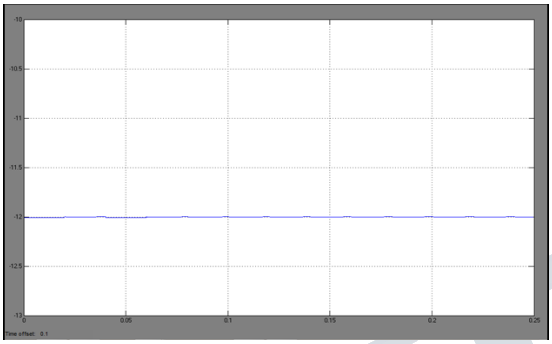

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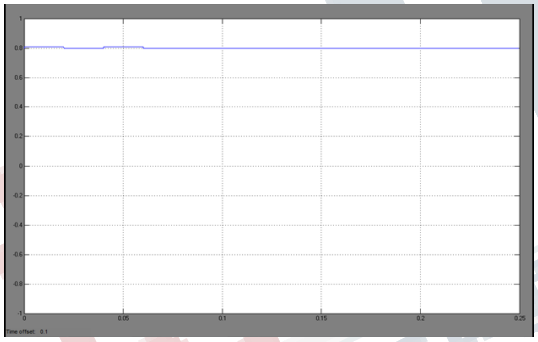
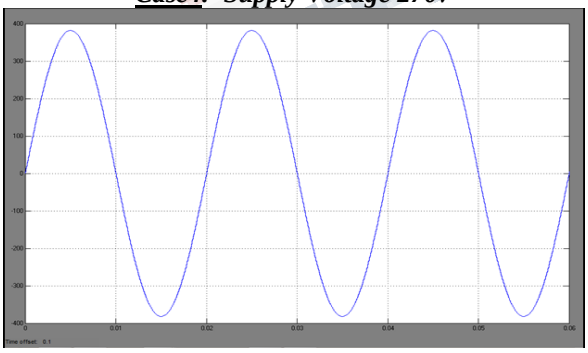


I04

***Case4:* Supply Voltage 270v**



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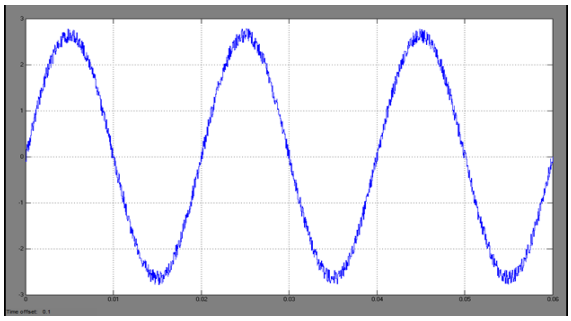

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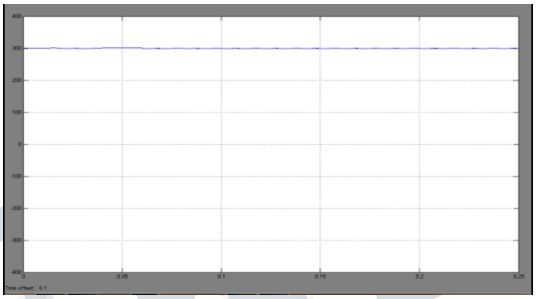

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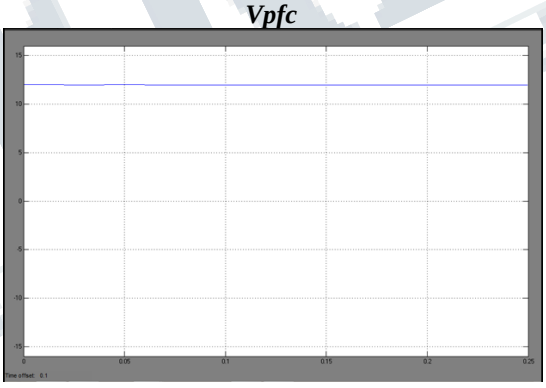

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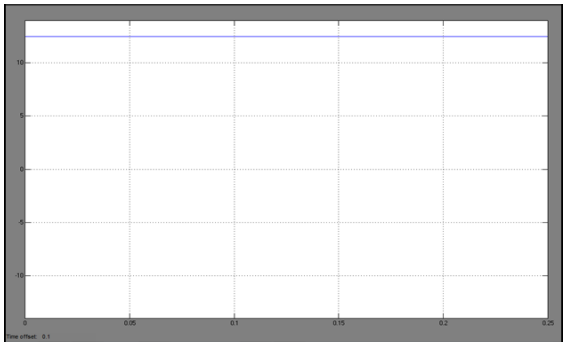

I01

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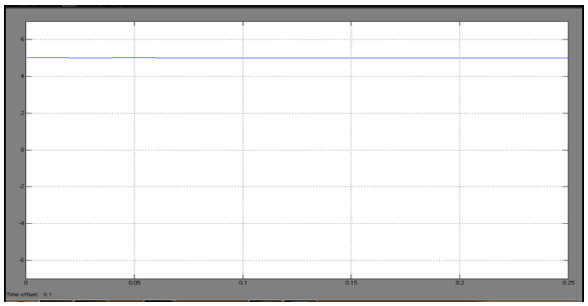

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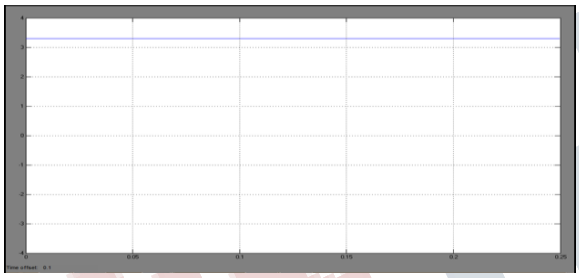

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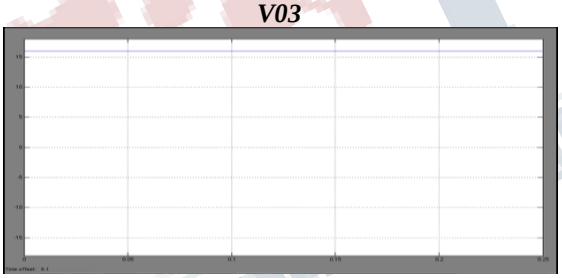

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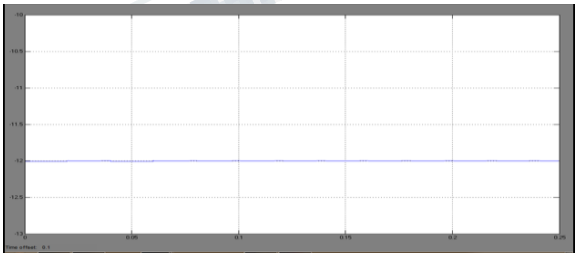

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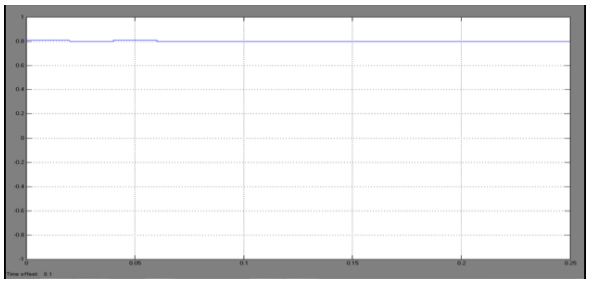

I04

THD	Proposed	Extension
Full load iac	3.33%	2.76%
Load changing Iac	3.76%	2.84%
Full load condition 170v Iac	4.30%	3.30%
Full load condition 270v Iac	2.71%	2.08%

V. CONCLUSION

A bridgeless non-secluded SEPIC based power supply has been proposed here to relieve the power quality issues pervasive in any regular PC control supply. The proposed control supply can work tastefully under wide varieties in info voltages and burdens. The outline and recreation of the proposed control supply are at first conveyed to exhibit its enhanced execution. Further, a research center model is constructed and examinations are directed on this model. Test comes about acquired are observed to be in accordance with the recreated execution. They confirm the way that the power quality issues at the front end are alleviated and subsequently, the proposed circuit can be a prescribed answer for PCs and other comparative machines.

In proposed paper, we implemented PI and fuzzy logic controller for bridgeless Converter Based Computer Power Supply. We compared the Total harmonic distraction (THD) for both PI and fuzzy logic controller. In Future, the same design can be implemented using Neural Network for more efficient output results.

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