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Digital Sigma Delta Modulators: An Overview

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***Abstract*- The audio devices use Sigma Delta DAC (Digital to Analog Converter) an essential block at the receiver side. This DAC has many blocks out of which noise shaping loop also known as Sigma Delta modulator is all digital circuit. The area and power consumption and speed of this block affect the performance of the entire DAC. There are various types of Sigma Delta modulators available. Different methods are developed for the performance improvement of these modulators. This paper discusses in detail various types of digital Sigma-Delta modulators and different performance improvement techniques available.**

***Keywords*: The area, delay, error feedback, MASH, power Sigma Delta DAC.**

I. INTRODUCTION

With the advancement in VLSI technology, the area, power and delay of electronic devices are reducing every day. The commonly used Audio devices like MP3 players, iPods, etc. needs to be less area, power consuming. These devices use Sigma Delta DAC which is a type of Oversampling converter. The basic types of converters available are Nyquist rate converters and Oversampling converters. The Nyquist rate converters sample the input signal at a frequency Fs, which is twice the frequency present in the input signal. The Oversampling converters sample the input at frequency Fs'= OSR * Fs, where OSR is Oversampling Ratio. This Oversampling DAC has an interpolator at the input side followed by noise shaping loop. The output of noise shaping loop is then given to the actual DAC and output of it is connected to the analog reconstruction filter. The interpolator and the noise shaping loop are digital circuits whereas the real DAC and reconstruction filter are the analog circuits [1]. The overall performance of the audio devices is mainly dependent on the performance of Sigma Delta DAC which is turn is dependent on noise shaping loop. The organization of the paper is as follows: Section 2 discusses in detail Sigma Delta DAC, section 3 elaborates various types of modulator, section 4 describes performance improvement techniques for the noise shaping loops and section 5 summarizes the conclusion of the work presented.

II. SIGMA DELTA DAC

The block diagram of Sigma Delta DAC is as shown in Fig. 1. The input received by the interpolation filter is a multi-bit data which is sampled near the Nyquist rate FS. The roles of interpolation filter are to raise the sampling frequency to OSR. FS and allow subsequent noise shaping and also to suppress the spectral replicas centered at FS, 2 FS, 3 FS, ..., (OSR-1) FS. The modulator reduces the word length of the input signal to only few bits. If a single-bit modulator is used, the linearity requirements of the internal DAC can be relaxed. If the output of the modulator is multi-bit, then to achieve linearity, techniques for cancelling the non-linearity errors of the DAC have to be used. In both the cases, the output of modulator will contain the truncation noise caused by the reduction of the word length in the modulator. If the input to internal DAC is a single bit, then its output will be a two level analog signal. The DAC structure, in case of single bit input, is straightforward, and its linearity is perfect. But, the high slew rate of the DAC output signal and a significant amount of out-of-band noise contained in it; make the design of analog filter difficult. But for a multi-bit DAC, additional circuitry is required for removing DAC non-linearity errors which result in more complex DAC. Finally, the analog reconstruction filter at the output of DAC removes most of the out-of-band noise contained in its input signal [1].

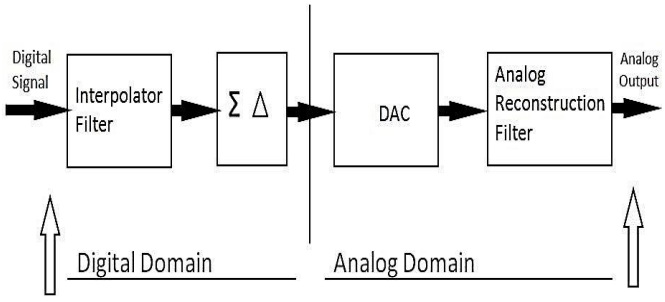

Figure 1. Block diagram of Sigma Delta DAC

III. NOISE SHAPING LOOPS

A wide variety of loop architectures is available for Sigma Delta DACs. The function of the noise shaping loop is to reduce the resolution of the input signal to a few bits without affecting its in-band spectrum. The reduction of word length

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means that the quantization or truncation error is introduced, the noise shaping loop must suppress the power spectrum of this added noise in the signal band. Some of the typical noise loop configurations are as follows:

1. Single stage Sigma Delta Loops
2. Error Feedback Structure
3. MASH Structures

3.1 Single stage Sigma Delta loops

The structure ontaining cascaded integrators with distributed feedback and input coupling (CIFB), the circuit using cascaded resonators with distributed feedback and input coupling (CRFB) as well as structures containing cascaded integrators or resonators with a feed-forward coupling (CIFF) as shown in the Fig. 2 to Fig. 5 are commonly used as single stage Delta Sigma loops. The component blocks are accumulators, and they are implemented using digital adder and multipliers [1]. Here the MSB (Most Significant Bit) which is retained in the output signal is feedback, and the LSBs (Least Significant Bit) are discarded.

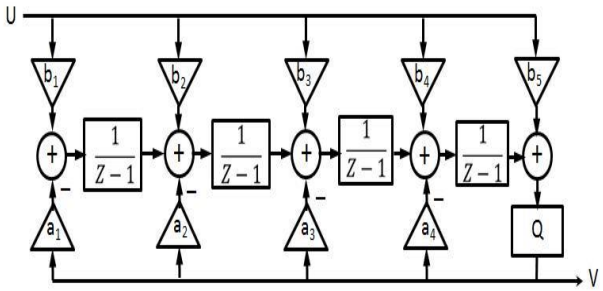

Figure 2. CIFB structure

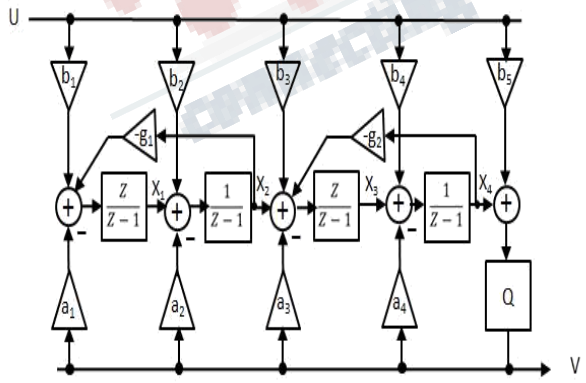

Figure 3. CRFB structure

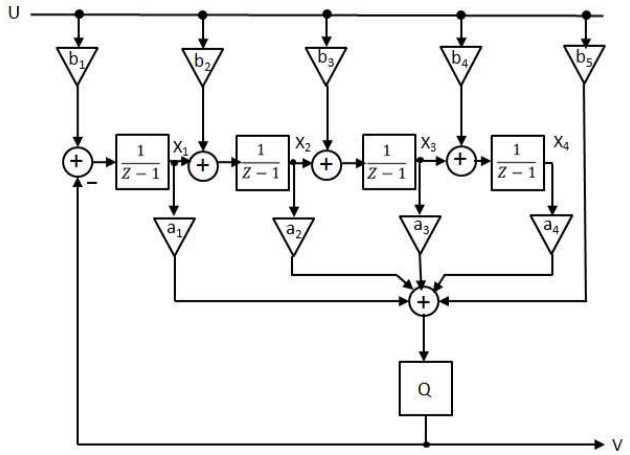

Figure 4. CIFF structure

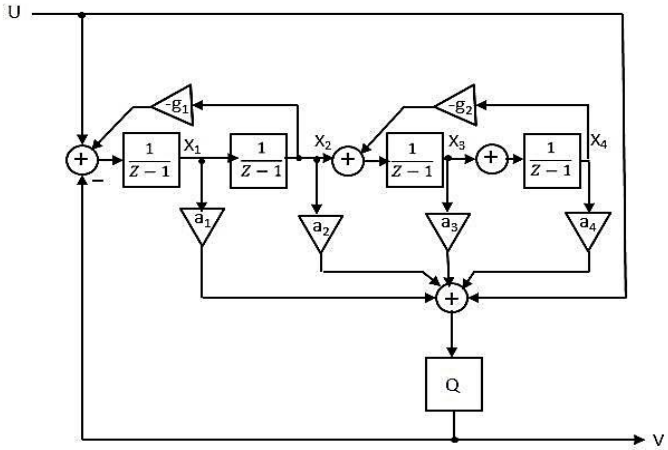

Figure 5. Modified CIFF structure

3.2 Error feedback structure

The general structure of a single quantizer Sigma Delta noise shaping is as shown in the Fig. 6. In this diagram, the noise shaping loop (modulator) is divided into two parts: a linear component (the loop filter) containing the memory elements and a memory less section (the quantizer). The loop filter is a two input system whose single output Y can be expressed as a linear combination of its inputs U and V:

$$Y(z) = L_0(z)U(z) + L_1(z)V(z) \qquad (1)$$

The operation of the quantizer is described as the addition of the error signal:

$$V(z) = Y(z) + E(z) \qquad (2)$$

Using equations 1 and 2, the output V can be written as a linear combination of two signals, the modulator input U and the quantization error E:

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$$V(z) = STF(z)U(z) + NTF(z)E(z) \quad (3)$$

Where

$$NTF(z) = \frac{1}{1 - L_1(z)} \quad and$$

$$STF(z) = \frac{L_0(z)}{1 - L_1(z)} \quad (4)$$

In the error feedback structure, rather than feeding back the MSB retained in the output, the discarded LSBs are filtered and fed back to the input. The loop filter He used to filter is located in the feedback path [1]. The error feedback structure is shown in the Fig. 7. The linear analysis of the circuit indicates that the output is given by:

$$V(z) = U(z) + [1 - L_1(z)]E(z) \quad (5)$$

Comparing equation 5 with 3, STF = 1 and NTF is $1 - H_e(z)$

For first-order loop, $NTF = 1 - z^{-1}$ and hence $H_e(z) = z^{-1}$ and is a simple delay circuit.

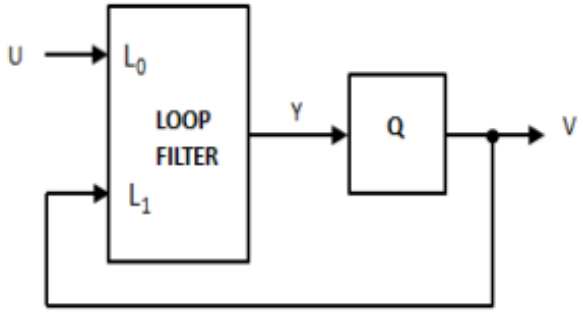

Figure 6. General structure of a single quantizer sigma-delta modulator

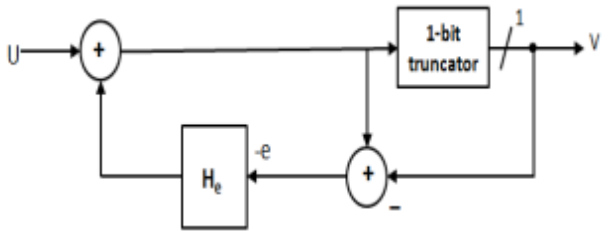

Figure 7. Error feedback structure

3.3 MASH structures

The basic concept of the cascaded modulator also known as Multi-stAge noise-Shaping (MASH) is shown in the Fig. 8. Here, the second stage is realized by another Delta Sigma modulator. The output signal of the first stage is given by:

$$V_1(z) = STF_1(z)U(z) + NTF_1(z)E_1(z) \quad (6)$$

where STF1 and NTF1 are the signal and noise transfer functions, respectively, of the first stage. The output of the first stage is then fed to another sigma delta loop forming the second stage of the modulator [1]. Therefore, the output of the second stage in the z-domain is given by:

$$V_2(z) = STF_2(z)E_1(z) + NTF_2(z)E_2(z) \quad (7)$$

where STF2 and NTF2 are the signal and noise transfer functions, respectively, of the second stage. The digital filter stages H1 and H2 at the output of the two modulator loops are designed such that in the overall output V(z) of the system the first stage error E1(z) is cancelled, this is possible if the condition:

$$H_1 NTF_1 - H_2 NTF_2 = 0 \quad (8)$$

is satisfied. Therefore, the most straightforward choice for H_1 and H_2 is $H_1 = STF_2$ and $H_2 = NTF_1$. The overall output is then given as:

$$V = H_1 V_1 + H_2 V_2 \quad (9)$$
$$V = STF_1 STF_2 U - NTF_1 NTF_2 E_2$$

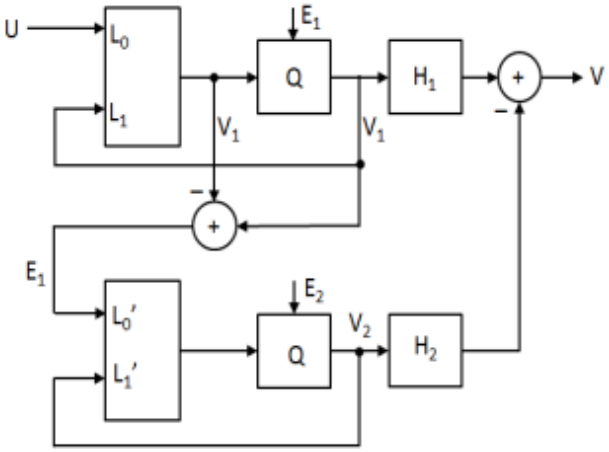

Figure 8. A two stage MASH structure

IV. PERFORMANCE IMPROVEMENT TECHNIQUES

The performance of modulator regarding area, power and delay affects the performance of the entire DAC device. There are primarily two different techniques used to improve the performance of these modulators. These techniques are namely: 1. Architecture based and 2. Gate level based.

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4.1 Architecture based

A lot of researchers have been working on different improvement techniques at the architecture level. A low power, low distortion Sigma Delta audio DAC for low output impedance audio applications utilized a modified 4th order inversed follow the leader feedback modulator for achieving high system performance [2]. The stereo audio DAC used an interpolation filter, 1-bit 4th order modulator and switched capacitor post filter to achieve low power and high resolution [3]. Experimental results were obtained for fourth order five bit error feedback loop. Hardware reduction of error feedback modulator was achieved by splitting the combinational circuitry of the modulators into two parts: one is producing the modulator output and another providing the error feedback signal [4]. Fourth order modulator implemented used 26% less area and 33% less dynamic power than the conventional techniques. A bus splitting technique for reducing the hardware complexity of digital Sigma-Delta modulators was reviewed and implemented on standard error feedback modulator architecture [5]. The same authors addressed error feedback modulators with DC inputs plus additive LSB dithering and showed how hardware reduction could be achieved. They also discussed error feedback modulators with sinusoidal inputs and demonstrated how bus splitting and error masking techniques could be used to obtain a trade-off between the modulator complexity and possible signal-to-noise ratio [6]. A reduced complexity third-order digital Sigma-Delta modulator for fractional-N frequency synthesis has been discussed [7]. The modulator consists of two sub-blocks where the first block is first-order error feedback structure and the second sub-block is a third-order new Ritchie structure. This reduced the hardware required for the implementation. MASH modulators are nowadays being researched extensively due to their inherent advantages. Nested Delta-Sigma modulator architecture for fractional-N frequency synthesis was investigated and compared with the conventional MASH 1-1-1 modulator. The nested structure required 15% lesser flip flops, 13% less full-adders and thus provided overall hardware saving of 15% [8]. Authors developed a design methodology for reducing the complexity of digital Delta-Sigma modulators. The design methodology based on error masking decreased hardware requirements of MASH modulators by up to 20% as compared to the conventional method [9]. The same authors proposed a design methodology for bus splitting MASH digital Delta-Sigma modulators based on error masking which exploits knowledge of the positions of the tones when the input is constant [10]. Using this technique hardware reduction of at least 13% could be achieved in the undithered case with constant input as compared to a standard architecture. A MASH 111 Delta-Sigma modulator is widely used in a fractional-N frequency synthesizer. A low complexity Delta-path design in a MASH 111 modulator by merely recoding all carry output signals from accumulators was presented [11]. Areduced complexity MASH digital Delta-Sigma modulator was introduced [12]. A long word was used for the first modulator in a MASH structure to maximize the sequence length, and shorter words were then used in subsequent stages. This structure performed better than the conventional MASH structure but with reduced hardware.

4.2 Gate level based

A lot of researchers have implemented the architectural level modifications to the modulator. Gate level based alterations in the modulator usually are complicated and are time consuming tasks. A single loop second order CMOS Sigma Delta modulator with reduced complexity, area reduction and low energy conversion was implemented for digital audio hearing aid applications [13]. The implementation of MASH 1-1 and MOD 2 (Error Feedback second order) digital modulators for Sigma Delta DACs was recently performed at gate level basis. A new digital circuit design technique known as Gate Diffusion Input (GDI) method was utilized for the two modulators. These two modulators were compared with those developed using static CMOS technology. The GDI based modulators performed well regarding area, power dissipation and power delay product as compared to the CMOS designs and also maintained the system performance [14].

V. CONCLUSION

Every electronic device today, needs to be efficient regarding area, power and speed. With VLSI field advancing, this efficiency for the devices can be very well achieved. This paper, presented types and improvement techniques of one of such frequently used device known as Sigma Delta modulator of Sigma Delta DAC. There are three main types of modulators and there are two crucial performance improvement techniques. The survey shows that there are many ways to perform architectural modifications in the modulator for improving the performance. But, there are very few ways are available to provide change at the gate level of the modulator.

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