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Study of Single Phase Multilevel Inverter for Pv Application

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***Abstract*: -- Solar photovoltaic modules are used to generate electricity from solar energy. The voltage generated during solar PV modules is DC in nature. However, most of the applications require AC quantities as input. Hence, multilevel inverters are employed to convert the DC voltage output of the PV module into AC voltage. In this paper, a detailed study of PV module is presented along with its modeling and simulation results showing the I-V and P-V characteristics obtained at different irradiance levels. The paper also includes the study of cascaded H-bridge inverter topology. Further, a comparative study is carried out between EPWM (Equal pulse width modulation) and SPWM (Sinusoidal pulse width modulation) techniques which enables to select the technique resulting in fewer harmonics for further simulations. The harmonic contents are determined with the help of FFT analysis in MATLAB.**

I. INTRODUCTION

The increasing use of electrical and electronic gadgets leads to the dernand for quality power. As the sources of conventional energy are limited we are in a search of newer techniques to use renewable energy in a very efficient and economic way. Solar energy is a better choice for electric converts solar energy directly into electrical energy. The photovoltaic array is formed using number of series and parallel modules of solar photovoltaic cell. The mathematical model of PV model is established using some assumptions with respect to the physical nature of the behavior of cell. The ideality factor of Si-poly is considered among the various technologies of PV cell. As AC power is needed in most of industrial and domestic applications, there is a need to convert DC output of PV module into AC. Multilevel inverter are required for this purpose. Multilevel inverter was introduced in 1957. The concept is to produce higher voltage output in small voltage steps by utilizing DC sources and switches. As the number of voltage steps increases the output waveform of the inverter approaches near to sinusoidal waveform . The equal pulse width modulation technique for five level multinverter is studied. The harmonic content was found to be very high i.e. 41.69%. In order to alleviate this problem sinusoidal pulse width modulation technique for gate pulse generations used. In this method, sinusoidal wave is used as reference and triangular wave as carrier wave. Phase opposition disposition scheme is used. The harmonic content level reduces to 26.8%. The simulation results are shown followed by conclusion.

II. STUDY OF PV MODULE

Single diode model of PV module is considered in this paper. A diode is connected with the light generated current source in anti-parallel. Here, in the model we have considered both series and parallel resistance[1]-[3]. The circuit model of a Photovoltaic cell is illustrated in Fig. 1

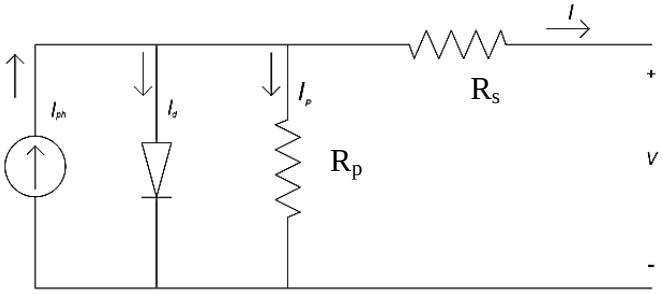

Fig. 1 The equivalent circuit of PV model with Rs and Rp.

The parameters used in the circuit model are:I_{ph} is pphotocurrent, I_d is diode current, I_p is current leak in parallel resistor. I is output voltage, R_s is series resistor and R_p is parallel resistor.

The equation of output current can be obtained by using Kirchhoff law,

$$I = I_{ph} - I_d - I_p \tag{1}$$

The output current of a module containing Ns cells in series in given in the equation (2)

$$I = I_{ph} - I_0\left[\exp\left(\frac{V + I.R_S}{a}\right) - 1\right] - \frac{V + R_s I}{R_p} \tag{2}$$

Where a is modified ideality factor and is given by

$$a = \frac{N_S \cdot A \cdot k \cdot T_C}{q} = N_S \cdot A \cdot V_T \tag{3}$$

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Where I_o is reserve saturation current V_{TL}=26mV at 300K for Silisium cell,T_c is the actual cell temperature, k is Boltzmann constant (1.381 × 10^{-23}J/K), q is the electron charge,V_T is called the thermal voltage.

A. Determination of I_{ph}:

The photocurrent is dependent on temperature and irradiance

$$I_{ph} = \frac{G}{G_{ref}}(I_{ph,ref} + \mu_{sc} \cdot .\Delta T) \quad (4)$$

Where G=Irradiance (W/m^2), Gref= Irradiance at STC=1000W/m^2,ΔT=Tc=Tref,Tref25+273=298K, μsc=coefficient temperature of Short circuit (A/k)

B. Determination of Io:

The reverse saturation current is given by following equation:

$$I_0 = I_{0,ref}\left(\frac{T_c}{T_{c,ref}}\right)^3 \exp\left[\left(\frac{q\varepsilon_G}{A \cdot K}\right)\left(\frac{1}{T_{c,ref}} - \frac{1}{T_c}\right)\right] \quad (5)$$

Where Ioref is reference reverse saturation current, :Material band gap energy (eV) (1.12 eV for Si).

C. Determination of I_{oref}:

I_{oref} can be given by following equation

$$I_0 = I_{SC,ref} \exp\left(\frac{-V_{oc,ref}}{a}\right) \quad (6)$$

Simulation of the PV Model:

Simulation of PV model is done after implementation of all equations on the MATLAB. I-V and P-V characteristics for R_s=0.45Ω andR_p=310.02Ω are shown in Fig.2 and Fig. 3

Under STC temperature, when irradiance is varied from 1000W/m^2 to 500W/m^2 then output current and power gets halved.

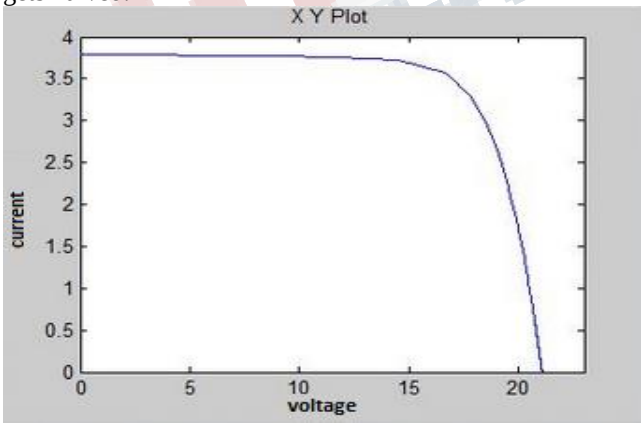

Fig. 2 I-V characteristics of PV cell.

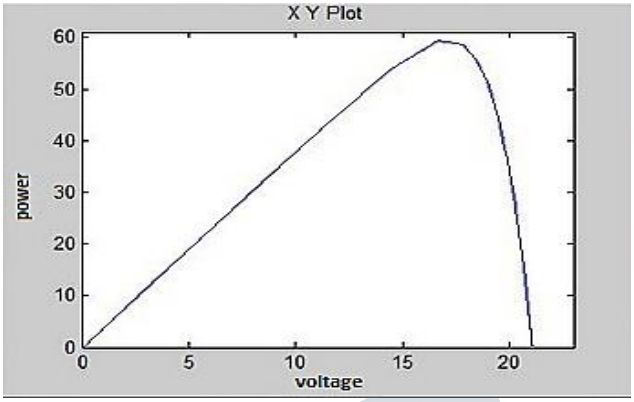

Fig. 3 P-V characteristics of PV cell.

The photovoltaic module is connected at the input of multilevel inverter. The output of PV module varies with the isolation level and depends on various other factors. But the multilevel inverter require constant output. To get a constant output from PV,use of MPPT(Maximum Power Point Tracker)technique becomes essential. In this paper cascaded H bridge topology of multilevel inverter has been considered for study purpose.

III. SYMMETRICAL CONFIGURATON (FIVE LEVEL INVERTER):

A. EPWM Technique:

1) Circuit Description:

Fig 4 shows the schematic circuit topology of the proposed five level multilevel inverter. It consists of two DC sources of voltage V. The number of H bridges is given by N = (m-1)/2, where 'm' is the number of levels. Thus, for 5 level inverter, two H bridges and hence eight switches are required. IGBTs are used as switches. In order to prevent the short circuit of the sources, simultaneous conduction of the switches (S1,S4), (S3,S2), (S5,S8), (S7,S6) must be avoided [4].

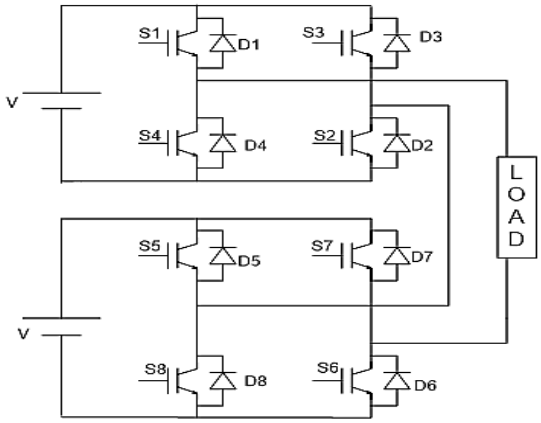

Fig. 4 Circuit diagram of five level inverter.

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2) Modes of Operation:

For one complete cycle, the circuit will be operated in five different modes that is two for positive half cycle, two for negative half cycle and one mode for zero level. In this way, one output voltage level is generated by each mode. Eight switching angles are needed which can be seen from the waveform as shown in Fig. 5 where the voltage levels are changing. Switching angles $\alpha = i*(180/m)°$ where i=1,2,….,(m-1)/2. 'i' varies from 1 to 2 for five level. Thus, α1 and α2 are found and all the remaining switching angles are determined from the symmetry of waveform.

α1=36°, α2=72°, α3 =180°-72°=108°, α4 =180°-36°=144° ,α5 =180°+36° =216°, α6 =180°+72°= 252°, α7= 360°-72°=288°, α9 = 360°-36°= 324°. (7)

Time delay of switching is given by,(α/360)*0.02 sec.

As α is 36°, for a particular voltage level particular switch is ON that that is pulse width of switch is 10%.

The switching state of switches for different voltage levels and time delay has been specified in switching table. Analysis of the circuit shows that for voltage level V, switches S1, S2 and S6 are ON. For voltage level 2V , along with S1, S2and S6 switch S5 is also ON. Width of pulse being 10%, in positive voltage level, switches S1, S2 and S6 have pulse width of 30% and S5 have pulse width of 10%. On similar lines, for negative voltages, pulse width of S7, S4 and S8 is 30% and that of S3 is 10%.

Fig. 5 Switching states of five level inverter.

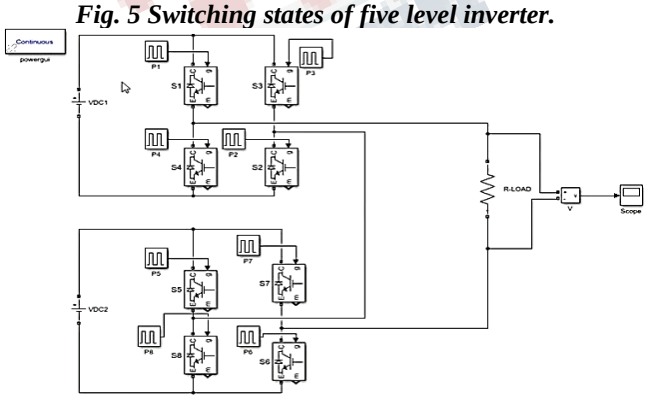

Fig. 6 Simulation circuitof five level inverter

PULSE NUMBER	0	V	2V	V	0	-V	-2V	-V	0
ANGLE (DEGREES)	36	72	108	144	216	252	288	324	360
TIME(SEC)	0.002	0.004	0.006	0.008	0.012	0.014	0.016	0.018	0.02
S1,S2&S6		ON PERIOD PUSLE WIDTH (30%)							
S3							10%		
S7,S4&S8						ON-PERIOD PULSE WIDTH (30%)			
S5			10%						

Table 1: Switching Table of five level inverter

3) Simulation Results:

The output waveform shows that the switches are operated according to the switching table, thus avoid short circuiting of sources. The total harmonic distortion is very high that is 41.69%. Odd harmonics are present n large amount with negligible even harmonics. As harmonics are responsible for the losses generated in the circuit, equal pulse methodology is replaced by sinusoidal pulse width modulation.

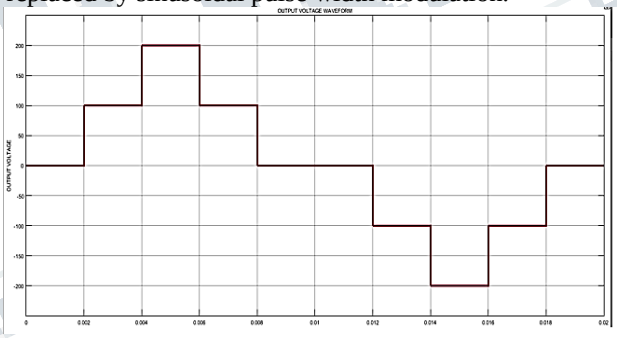

Fig. 7 Output waveform of five level inverter

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Sampling time     = 0.000338983 s
Samples per cycle = 59
DC component      = 8.682e-08
Fundamental       = 144.2 peak (102 rms)
THD               = 41.69%

   0 Hz   (DC):     0.00%   270.0°
  50 Hz  (Fnd):   100.00%    -0.0°
 100 Hz   (h2):     3.62%     0.0°
 150 Hz   (h3):    31.86%   180.0°
 200 Hz   (h4):     0.75%   180.0°
 250 Hz   (h5):     0.05%     0.0°
 300 Hz   (h6):     1.03%    -0.0°
 350 Hz   (h7):    15.22%   180.0°
 400 Hz   (h8):     3.69%   180.0°
 450 Hz   (h9):     9.70%    -0.0°
 500 Hz  (h10):     0.52%   180.0°
 550 Hz  (h11):    10.29%    -0.0°
 600 Hz  (h12):     3.75%     0.0°
 650 Hz  (h13):     6.61%   180.0°
 700 Hz  (h14):     0.55%   180.0°
 750 Hz  (h15):     0.15%     0.0°
 800 Hz  (h16):     1.44%    -0.0°
 850 Hz  (h17):     7.02%   180.0°
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Fig. 8 Simulation results of five level inverter

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B. SPWM Technique:

1) Introduction to SPWM:

Sinusoidal PWM is a method of generating gate pulses which uses phase-shifting technique to reduce harmonics in load voltage. The sinusoidal waveform is used as reference and triangular waves are used as carrier waves. For 'm' level inverter, 'm-1' carrier waves are required[5].The carriers used can be vertically shifted or horizontally shifted. But vertically shifted scheme is easy to implement in any digital controller and hence, is more popular. The vertically shifted schemes are classified as:

a) All the carriers are in phase (PH disposition)

b) The carriers above the zero level are in phase but are opposite to those below the zero level (PO disposition)

c)The carriers are in opposition alternatively (APO disposition)[5].

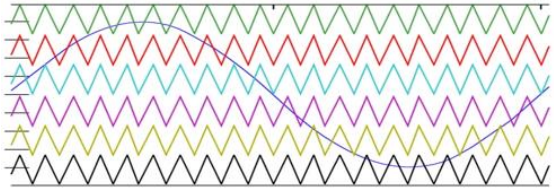

Fig. 9 Phase disposition

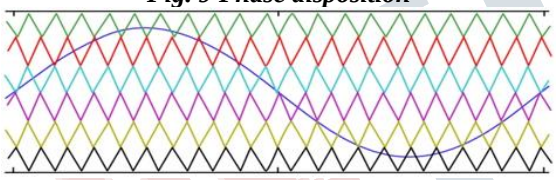

Fig. 10 Alternate phase opposition disposition

The phase opposition disposition (PO disposition) scheme was used to obtain gate signals for the switches of the multilevel inverter topology under consideration.

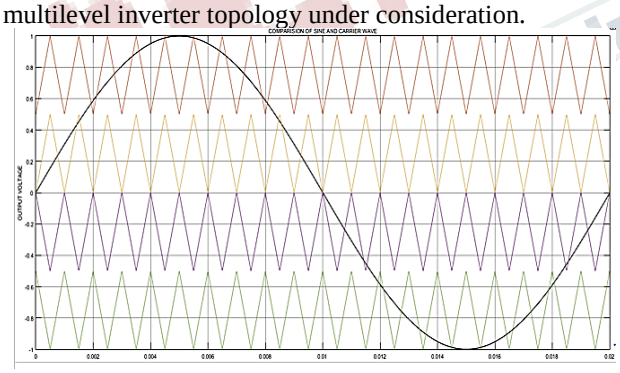

Fig. 11Phase Opposition disposition

2) Implementation of 5 Level Inverter using SPWM:

The topology used remains same that is shown in Fig. 4. Gate pulses to the switches are generated using SPWM technique. The amplitude modulation index for 5 level PO disposition SPWM is given below:

$$Ma=A_m/2A_c \quad (8)$$

where, Ac is the peak-peak value of carrier wave in pu (per unit) and Am is the peak value of the modulating wave in pu. For the simulation , the values chosen for Ac and Am are 0.5V and 1V respectively. Hence, the amplitude modulation ind ex becomes equal to 1.

The topology seen in Fig. 12 consists of two sources V_1 and V_2 ,each of 100V , and 8 switches are used. In the subsystem, the sine wave and the carrier waves are compared and their output is taken out. As there are four carrier waves, four comparisons are made and thus,four outputs are obtained. These outputs are given as gate signal to the switches S_1,S_2,S_5 and S_6.According to the basics, two switches in the same leg should not conduct at the same time. Hence, the remaining switches are given gate pulse from the same outputs but via NOT gates.

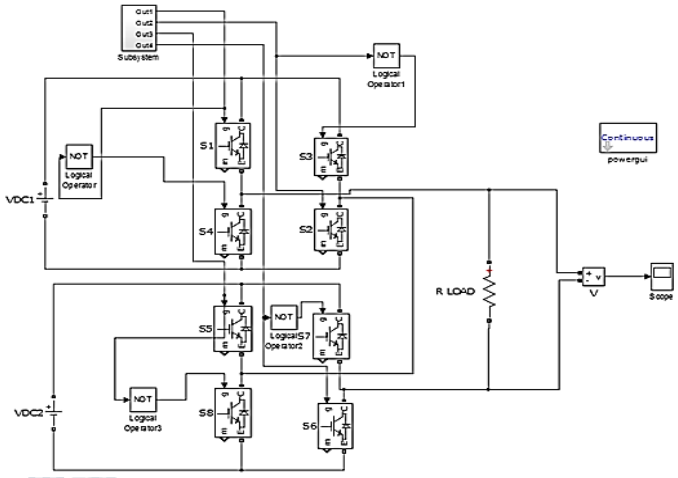

Fig. 12 Simulation model of 5 level inverter.

The five levels obtained at the output are 2V, V, 0,- V,- 2V.Table 2 is the switching table where S1 to S8 are the switches and 2V,V, etc. are the levels at the output. The entry '1' in the table indicates that the particular switch is in conduction for the specified output level. The output obtained for five cycles is shown in Fig. 13.

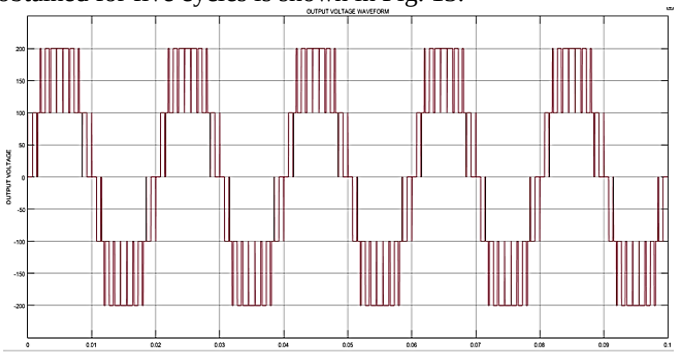

Fig. 13 Five level output of the inverter.

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Table 2 Switching table for 5 level output.

	S1	S2	S3	S4	S5	S6	S7	S8
2Vdc	1	1	0	0	1	1	0	0
Vdc	0	1	0	1	1	1	0	0
0+	0	1	0	1	0	1	0	1
0-	1	0	1	0	1	0	1	0
-Vdc	1	0	1	0	0	0	1	1
-2Vdc	0	0	1	1	0	0	1	1

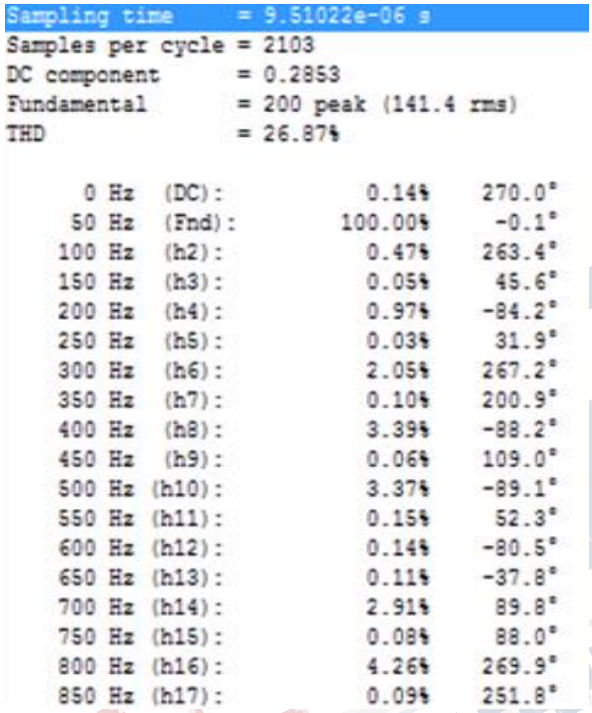

Fig .14 THD Analysis of five level inverter.

Table 3 shows the THD (Total Harmonic Distortion) analysis. When SPWM technique is used, the lower order odd harmonics are almost zero. The THD obtained in this method is 26.87% which is less than that obtained in fundamental switching method. Thus, SPWM is preferred over fundamental switching method.

V. CONCLUSION

A detailed modeling and simulation of the PV module is presented in this paper. It is implemented under MATLAB simulink environment.. The comparison is made between EPWM (equal pulse width modulation) and SPWM (sinusoidal pulse width modulation) which shows that the THD (total harmonic distortion) obtained is less when SPWM is used.

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