ISSN (Online) 2456-1290
International Journal of Engineering Research in Mechanical and Civil Engineering (IJERMCE)
Vol 1, Issue 4, August 2016

Design of a PID Controller for an Improved SEPIC Converter for SPV System

[1]Dileep. G, [2]S. N. Singh
[1] Research Scholar, [2] Senior Scientific Officer,
Alternate Hydro Energy Centre, Indian Institute of Technology Roorkee, Uttarakhand-247667
[1] dileepmon2@gmail.com

***Abstract*— This paper describes the design of a Proportional Integral Derivative (PID) controller for a new switched inductor (SI) based single ended primary inductance (SEPIC) converter working in Continuous Conduction Mode (CCM). The main objective is to obtain a stable, robust and controlled system by tuning the PID controller. A state space average model of SI-SEPIC has been developed and by exact tuning method the parameters of PID Controller are obtained. The converter operates at a switching frequency of 50 kHz. MATLAB/Simulink based simulation results are presented to validate the design procedure.**

***Index Terms*— PID Controller, SEPIC converter, bode plot, XACT tuning method.**

I. INTRODUCTION

Renewable energy resources such as wind energy, solar energy, hydro energy etc. are used as sources for many distributed generator (DG) systems. Power conversion is an essential requirement for DG systems since most of renewable energy resources are variable in nature. For example, Variable voltage and variable frequency output wind turbine system need to be converted into a fixed voltage and fixed frequency ac output feeding into a grid. Photovoltaic (PV) panel produces variable dc output which is to be converted into a fixed voltage for domestic and industrial applications. Power converters have been used to accomplish this power conversion function. Hence power converter is a critical component of a DG system. With the rapid development and growing applications of DG systems, power converters have evolved from a traditional "power conversion device" to a "system integrator". The high power step up dc-dc conversion technique finds increasing necessities and power capability demands in applications such as UPS, electric vehicles and photovoltaic system where the low dc input voltage must be converted into higher dc output voltage. Selection of DC-DC converters for solar power tracking is based on certain factors such as efficiency, cost, PV module effect, input/output energy flow and flexibility. Boost converter, Buck converter, Buck-Boost converter, Single ended primary inductor converter (SEPIC) and Cuk converter are commonly used for power tracking. Boost converter [1] is used to step up the input voltage while buck converter [2] is used for step down the input voltage. Buck-boost, cuk and SEPIC converter performs both bucking and boost action. Output voltage of buck-boost [3] and cuk converters [4] are inverted while SEPIC converter[5] provides non inverted output voltage with continuous input/output energy flow and better efficiency. Hence a SEPIC converter is preferred over other converters. Output voltage regulation in the dc-dc converter is achieved by adjusting the duty cycle with the help of PID controller [6] PID controller is the combination of PD and PI controller. The PID controller algorithm involves three separate constant parameters i.e P,I & D. PID controller operates directly on error signal which is the between desired output and actual output. By tuning the three parameters in the PID controller algorithm, the controller can provide control action designed for specific process requirements. The response of the controller can be described in terms of the responsiveness of the controller to an error, the degree to which the controller overshoots the set point, and the degree of system oscillation.

To investigate these design issues, the state space average model, transfer function and bode plot of proposed converter will be established in Section II. In Section III, the proposed digital PID controller using exact tuning method [7] for proposed SI-SEPIC converter will be presented. Section IV will present the MATLAB/Simulink model to verify the system responses system responses. Finally, some conclusions are described in Section V.

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II. OPERATION OF SI-SEPIC CONVERTER

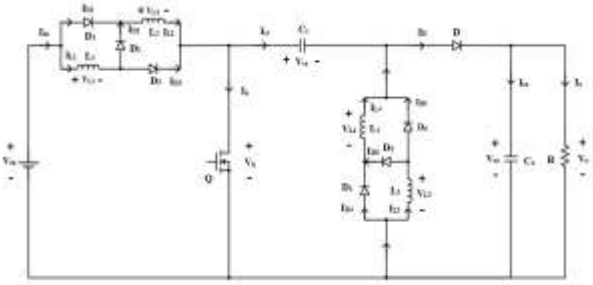

Fig. 1: Circuit diagram of SI-SEPIC converter.

a. State Space Average Model

Circuit diagram of the proposed SI-SEPIC converter is shown in Fig. 1. Input and output side inductors of the conventional SEPIC converter are replaced with switched inductor structures in order to increase the gain. Design of converter is done in such a way that all the inductors charge simultaneously when the switch is ON and discharge simultaneously when the switch is OFF. The operation of the proposed converter is symmetrical in two half-line cycles of the input voltage; hence, converter operation during one switching period in positive half-line cycles of the input voltage is explained here. It is assumed that the converter operates in CCM. All the circuit elements are assumed to be ideal, and it is supposed that the converter is operating under steady state. Output capacitor, C_o is assumed to be large enough to reduce the output voltage ripple.

MODE: 1 (0 < t <DT): Mode 1 starts when the switch Q is turned on, diodes D_1, D_3, D_4 and D_6 are forward biased and diodes D_2, D_5 and D are reverse biased. V_{in} starts charging inductors L_1 and L_2 in parallel. During this stage, energy stored in the coupling capacitor is transferred to inductors L_3 and L_4. Equivalent circuit of SI-SEPIC converter during ON period is shown in Fig. 2.

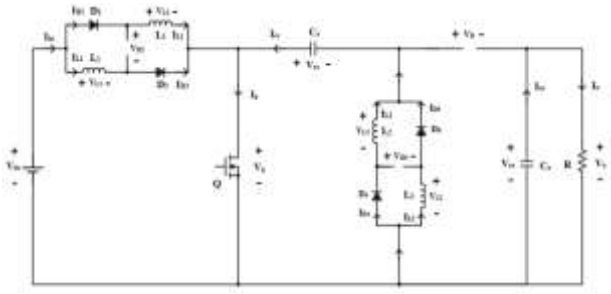

Fig. 2. Equivalent circuit when switch is ON.

During switch ON: Applying KCL and KVL, state equations of the proposed converter are given by Eq. (1) to Eq. (4),

$$\frac{di_{La}}{dt} = \frac{V_{in}}{L_a} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$\frac{dV_{cs}}{dt} = -\frac{I_{Lb}}{C_s} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

$$\frac{di_{Lb}}{dt} = \frac{V_{cs}}{L_b} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

$$\frac{dV_{co}}{dt} = -\frac{V_{co}}{RC_o} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

State equations for ON period are expressed in state space form as given in Eq. (5) and Eq. (6),

For ON period La is equivalent inductance of parallel combination of L_1 and L_2 and L_b is equivalent inductance of parallel combination L_3 and L_4 as shown in Fig. 2.

MODE: 2 (DT < t <T): Switch is turned OFF, diodes D_2, D_5 and D are forward biased and diodes D_1,D_3,D_4 and D_6 are reverse biased. Energy stored in inductors L_1 and L_2 is transferred to coupling capacitor. Energy stored in inductors L_3 and L_4 along with V_{in} is transferred to load through diode D.

$$\begin{bmatrix} \frac{di_{La}}{dt} \\ \frac{dV_{c_s}}{dt} \\ \frac{di_{L_b}}{dt} \\ \frac{dV_{c_o}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C_s} & 0 \\ 0 & \frac{-1}{L_b} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{RC_o} \end{bmatrix} \times \begin{bmatrix} i_{La} \\ V_{c_s} \\ i_{Lb} \\ V_{c_o} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_b} \\ 0 \\ 0 \\ 0 \end{bmatrix} \times V_{in} \quad \ldots (5)$$

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$$V_o=\begin{bmatrix}0 & 0 & 0 & 1\end{bmatrix}\times\begin{bmatrix}i_{L_a}\\ V_{c_s}\\ i_{L_b}\\ V_{c_o}\end{bmatrix} \quad \ldots\ldots\ldots\ldots \quad (6)$$

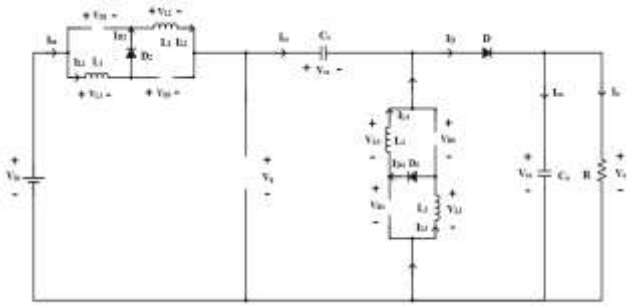

Fig. 3. Equivalent circuit when switch is OFF.

During switch OFF: Applying KCL and KVL, state equations of the proposed converter are given by Eq. (7) to Eq. (10),

$$\frac{di_{La}}{dt}=\frac{V_{in}-V_{cs}-V_{co}}{2L_a} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (7)$$

$$\frac{dV_{cs}}{dt}=-\frac{I_{La}}{C_s} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (8)$$

$$\frac{di_{Lb}}{dt}=\frac{V_{co}}{L_b} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (9)$$

$$\frac{dV_{co}}{dt}=\frac{I_{La}}{C_o}-\frac{I_{Lb}}{C_o}-\frac{V_{co}}{RC_o} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (10)$$

State equations for ON period are expressed in state space form as given in Eq. (11) and Eq.(12),

For OFF period La is equivalent inductance of series combination of L_1 and L_2 and L_b is equivalent inductance of series combination L_3 and L_4 as shown in Fig. 3.

$$\begin{bmatrix}\frac{di_{L_a}}{dt}\\ \frac{dV_{c_s}}{dt}\\ \frac{di_{L_b}}{dt}\\ \frac{dV_{c_o}}{dt}\end{bmatrix}=\begin{bmatrix}0 & \frac{-1}{2L_a} & 0 & \frac{-1}{2L_a}\\ \frac{1}{C_s} & 0 & 0 & 0\\ 0 & 0 & 0 & \frac{-1}{2L_b}\\ \frac{1}{C_o} & 0 & \frac{1}{C_o} & \frac{-1}{RC_o}\end{bmatrix}\times\begin{bmatrix}i_{L_a}\\ V_{c_s}\\ i_{L_b}\\ V_{c_o}\end{bmatrix}+\begin{bmatrix}\frac{1}{2L_a}\\ 0\\ 0\\ 0\end{bmatrix}\times V_{in} \quad (11)$$

And,

$$V_o=\begin{bmatrix}0 & 0 & 0 & 1\end{bmatrix}\times\begin{bmatrix}i_{L_a}\\ V_{c_s}\\ i_{L_b}\\ V_{c_o}\end{bmatrix} \quad (12)$$

Transfer function of SI-SEPIC converter

Output to input transfer function of SI-SEPIC converter is given by,

$$X(s)=B(SI-A)^{-1}C+E \quad (13)$$

Substituting for system matrix A, input matrix B, output matrix, C and direct transmission matrix, E in Eq. (14), output to input transfer function of SI-SEPIC converter is obtained as,

$$\frac{V_o}{V_{in}}=\frac{1875(s^2+5*10^8)}{s^4+0.01s^3+87500s^2+375*10^4 s+3.1*10^8}$$

Bode plot of the proposed converter

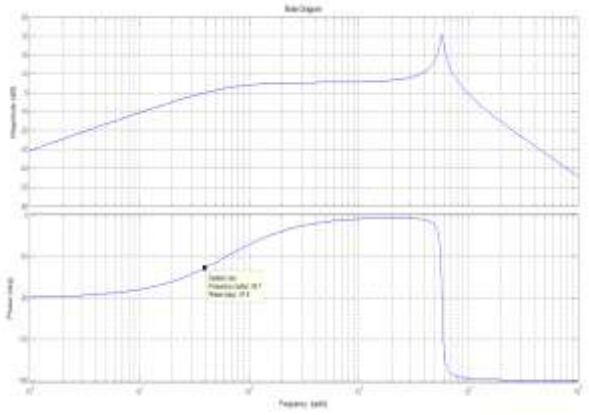

Fig.4. Bode plot of the proposed converter

Magnitude and phase plot of the proposed SI-SEPIC converter is shown in Fig. 4. From the plot, it is clear

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that the phase angle never crosses -180 degree, and hence gain margin of the proposed converter is infinity. phase margin of the proposed converter is 122.40 degrees. For a system to be stable both gain margin and phase margin must be greater than zero. For the proposed converter gain margin is infinity and phase margin is 122.4 degrees, since both these values are positive, the proposed converter is stable.

III. EXACT TUNING OF PID CONTROLLER DESIGN

Transfer function for a PID controller is given as,

$$C_{PID} = K_P(1+\frac{1}{T_i s}+T_d s) \quad \text{.....(15)}$$

In polar form, equation can be written as,

$$C_{PID}(j\omega) = M(\omega)e^{j\varphi(\omega)} \quad (16)$$

Plant can be represented in polar from,

$$G(j\omega) = |G(\omega)|e^{\angle j\varphi(\omega)} \quad (17)$$

Loop transfer function including PID controller and plant is given by,

$$G(j\omega) = |G(\omega)|M(\omega)e^{\angle j(\varphi(\omega)+\varphi(\omega))} \quad (18)$$

Parameters for the PID controller can be calculated as follows,

Proportional gain,

$$K_P = M_g \cos\phi_g \quad (19)$$

Integral time constant,

$$T_i = \frac{\tan\phi_g + \sqrt{\tan^2\phi_g + 4\sigma}}{2\omega_g} \quad (20)$$

Derivative time constant,

$$T_d = T_i\sigma \quad (21)$$

where, $M_g = M(\omega_g)$ (22)

$$\phi_g = PM - \pi - \angle G(\omega) \quad (23)$$

Maximum overshoot (OS) of the proposed converter is designed to be 1%, damping ratio and desired phase margin can be determined by eqn. (24) and eqn. (25)

Desired damping ratio,

$$\gamma = \frac{-\ln(\frac{\%OS}{100})}{\sqrt{\pi^2+\ln^2(\frac{\%OS}{100})}} = 0.91 \quad (24)$$

Desired phase margin,

$$\phi_g \cong \gamma * 100 = 91^0 \quad (25)$$

From bode plot, steady state gain is found to be 30 dB, gain cross over frequency, f_c=13Hz and degree of freedom σ is chosen as 5, which is the ratio of integral time constant to differential time constant. Substituting values in eqn (19-23), gain parameters can be determined as, σ

$$K_P = 19.29, K_I = 725, K_D = 2.5$$

IV SIMULATION RESULTS

Simulation test of the proposed SI-SEPIC converter shown in Fig. 1 was conducted using MATLAB/simulink to validate the theoretical analysis and measure the performance of the converter. Specifications of the converter used for simulation are as follows; L_1= L_2= L_3=L_4=18µH, C=60µF, C_o=200µF, f_s=50KHz, Po=114W and ESR of capacitor and inductor 20mΩ. Simulation results of the proposed converter for an input voltage of 14 V are shown in the Fig.5.

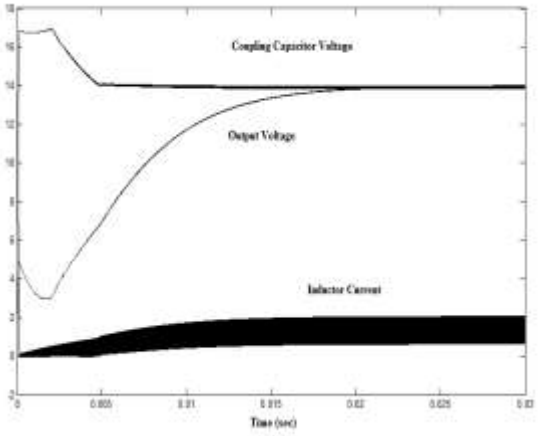

Fig. 5. Simulation results

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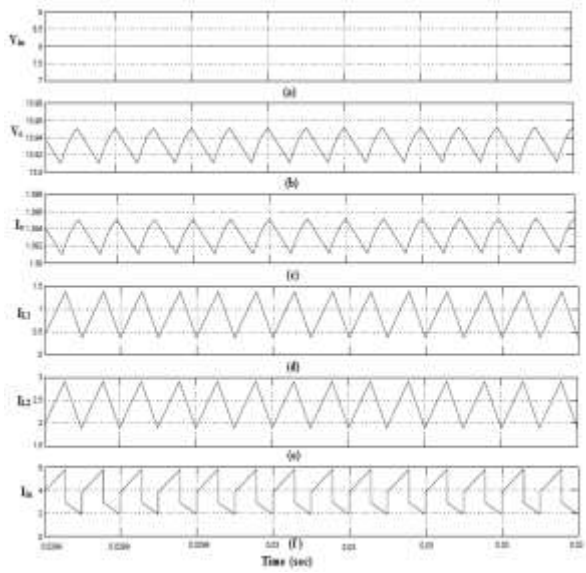

Fig. 6. Simulation results of the (a) input voltage, V_{in}, (b) Output voltage V_o, (c) Output current, I_o, (d) Inductor current, I_{L1}, (e) Inductor current, I_{L1} and (f) Input current, I_{in} for each switching period with Vin= 14V.

It is evident from the figure that the output of the proposed converter output voltage is maintained to 14 V within 0.02 seconds. Voltage across the coupling capacitor is 14 V which is equal to input voltag. Simulation waveforms of the proposed converter show good agreement with theoretical predictions. Coupling of inductors reduces the ripple in input current. The dynamic performance under input voltage change, load change and duty cycle changes has been investigated. Proposed converter was able to provide an output voltage which is twice that provided by conventional SEPIC converter under all conditions. In this paper, PID controller for the converter is designed for charging a 14V battery, which is used for standalone applications. Output voltage, output current, inductor current and input current for input voltage of 8 V is shown in Fig.6. Average value of output voltage is 13.94 V and output voltage ripple is 0.04 V. Inductor current ripple is 0.5 A.

V. CONCLUSION

The paper comprehensively describes the detailed design procedure of a PID controller for an improved SI-SEPIC converter which is derived from the bode plot. By applying the exact tuning method the PID controller was designed and for any change in the input voltage the output remains constant and hence the design of the controller is optimum. With PID controller there is a substantial improvement in the time domain specification in terms of lesser rise time, peak time, settling time as well as a lower overshoot. Proposed SI-SEPIC converter is stable under all conditions, and able to improve the overall gain.

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