ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 3, March 2017

Review on QSD Multiplier Design Using VHDL

[1] Pooja s. Rade, [2] Ashwini M. Khode, [3] Rajani N. Kapse, [4] Ankita M. Sor, [5] Smruti G. Bhasme
[5] Prashant Y. Shende
[1-5] BE 4th Year Student and [6] Assistant Profesor
[1-6] Department of ENTC, DMIETR Wardha, Maharashtra, India.

Abstract: **-- The need for high speed digital circuits became more prominent as portable multimedia and communication applications incorporating information processing and computing. In binary number system carry is a major problem in arithmetical operation including propagation delay and circuit complexity. To overcome this problem signed digit is required for carry free arithmetical operation. Further, literature reviews suggest that multi-valued logic (MVL) would be a better choice to address the problem of developing faster chips to perform faster computational operation. Quaternary Signed Digit (QSD) have major advantages in carry free arithmetical operation This paper is about a new number system for ALU. Carry free addition circuit is used to enhance the speed of operation. The design is structured for m × n multiplication where m and n can reach up to 126 bits. In this paper, we are giving the review of papers for the QSD multiplier.**

Keywords: **VHDL; QSD (Quaternary Signed Digit); Programmable Logic; Fast Computation.**

I. INTRODUCTION

In various computers & other processors, multipliers are implemented in ALUs and also in other portions of processors for calculating the address, table indices & same kind of operations. In the cases were negative numbers are presented through two's or one's complement, it is necessary to transform an adder, multiplier to Some other signed number presentations. QSD Adder / QSD Multiplier circuits are logic circuits designed to perform high-speed arithmetic operations. In QSD number system carry propagation chain are eliminated which reduce the computation time substantially, thus enhancing the speed of the machine.

II. QSD NUMBER SYSTEM

Quaternary is the base 4-numeral system. It uses the digits 0, 1, 2 and 3 to represent any real number. It shares with all fixed-radix numeral systems. It has the ability to represent any real number with a canonical representation (almost unique) and the characteristics of the representations of rational numbers and irrational numbers. See decimal and binary for a discussion of these properties.

Relation to binary

Quaternary has a special relation to the binary numeral system. Each radix 4, 8 and 16 is a power of 2, so the conversion to and from binary is implemented by matching each digit with 2, 3 or 4 binary digits, or bits. QSD numbers are represented using 3-bit 2's complement notation. To produce a appropriate decimal representation, each number can be represented by

$$D = \sum_{i=0}^{n-1} x_i 4^i$$

Where, x_i can be any value from the set $\{\bar{3}, \bar{2}, \bar{1}, 0, 1, 2, 3\}$
A QSD negative number is the QSD complement of the QSD positive number i.e., $\bar{3} = -3$, $2 = -2$ and $\bar{1} = -1$.
For example,

$$1\bar{2}\,\bar{3}\,\bar{3}_{QSD} = 1 * 4^3 + \bar{2} * 4^2 + \bar{3} * 4^1 + \bar{3} * 4^3$$
$$= 23_{10}$$

and $\bar{1}23\bar{3}_{QSD} = -23_{10}$

Comparison of QSD with BSD

It offers the advantage of reduced circuit complexity, i.e. number of transistor required is less and minimum interconnections are needed. According to this theorem QSD number uses 25% less space than BSD to store number. Theorem is described as under- to represent numeric value N, $\log_4 N$ number of QSD digits and 3 $\log_4 N$ binary bits are required. And for BSD representation of same number $\log_2 N$ BSD digits and 2 $\log_2 N$ binary bits are required. The ratio of number of bits required in QSD representation to the number of bits required in BSD representation for an any number N is

$$\frac{|3\ \log_4 N|}{|2\ \log_4 N|} = \frac{3\frac{\log N}{\log 4}}{2\frac{\log N}{\log 2}} = \frac{3}{2}\frac{\log 2}{\log 4} = \frac{3}{4}$$

Therefore, QSD saves ¼ of the storage used by BSD. Also it Reduce the computation time. In general the number of bits required by a QSD number system is less when compared to BSD number system, which in turn results in better speeds and performance.

III MULTIPLIER DESIGN:

There are generally two methods for a multiplication operation: parallel and iterative. The

All Rights Reserved © 2017 IJERECE

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 3, March 2017

multiplication of two whole numbers is equivalent to the addition of one of them with itself as many times as the value of the other one.

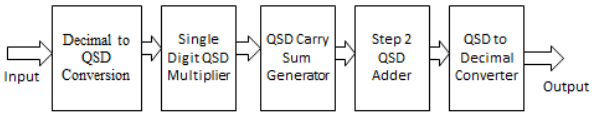

Figure.1 General Block Diagram of QSD Multiplier

There are total three steps required for QSD multiplication as shown in figure 1 above the basic block diagram for QSD multiplication. First step is the single digit partial product generator. After generating partial product in the form of Ci and Mi output form there is a generation of an intermediate carry and sum from the addend and augend. And the third step is the Second step QSD adder which adds the output of second step. Which combines the intermediate sum of the current digit with the carry of the lower significant digit. The n digit QSD multiplier shown below in figure 2.

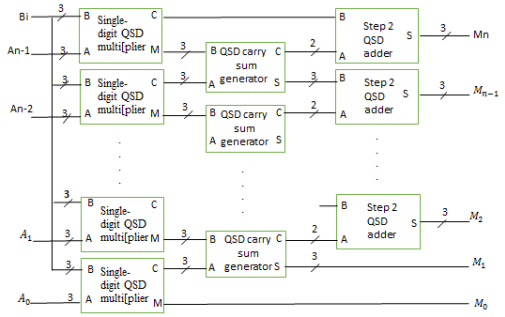

Figure 2: n-Digit QSD Multiplier

To avoid carry propagation delay. There are two rules are defined, the first rule is that the sum of the intermediate adder should not be greater than or equal to 2 and the second rule is that the carry should not be greater than 1. Thus by considering these rules we have to select minimal term for the QSD representation. Thus table 1 below shows that the QSD representation of the number in multiple ways and the selected QSD number used for codding in the last column.

Table1: QSD Number Representation for Carry free Addition and Multiplication

Sum and product	QSD represented number	QSD coded number
-9	$\bar{2}\,\bar{1}, \bar{3}3$	$\bar{2}\,\bar{1}$
-6	$\bar{1}2$, $\bar{2}\,2$	$\bar{1}\,\bar{2}$
-5	$\bar{2}\,\bar{3}, \bar{1}\,\bar{1}$	$\bar{1}\,\bar{1}$
-4	$\bar{1}0$	$\bar{1}0$
-3	$\bar{1}1$, $0\bar{3}$	$\bar{1}1$
-2	$\bar{1}2$, $0\bar{2}$	$0\,\bar{2}$
-1	$\bar{1}3$, $0\,\bar{1}$	$0\,\bar{1}$
0	00	0 0
1	01 , $0\bar{3}$	0 1
2	02, $1\,\bar{2}$	0 2
3	03, $1\,\bar{1}$	$1\,\bar{1}$
4	10	1 0
5	11, $2\bar{3}$	11
6	12 , $2\bar{2}$	12
9	21, $3\bar{3}$	21

III LITERATURE REVIEW

In 2011 Kothuru .Ram Kumar [et.al] presented a paper for the speed of computation which is restricted by generation & propagation of carry particularly with increment in quantity of bits. The processes like borrow free subtraction carry free addition & multiplication can be performed through implementation of QSD. Even though, some other logical components based over prime modules are needed for execution of arithmetic functions. An arithmetic function which is carry free is attained through higher radix number system like QSD. In QSD, every digit is presented in range of -3 to 3. This also helps in implementation of complex functions like carry free addition over large bit numbers like 64, 128 or more with persistent delay & low complicacy. Microwind, Modelsim6.0 & Leonardo Spectrum are used in synthesis & simulation of design.

In 2009 Reena Rani [et.al] presented a paper for executing the functions like addition, subtraction & multiplication with propagation delay. A higher radix number system like QSD helps in attaining carry free operation. Some fast speed adders constituted over QSD umber system are proposed in this paper. Every figure is presented through a number from range of -3 to 3 in the QSD. Operations like carry free addition &

All Rights Reserved © 2017 IJERECE

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 3, March 2017

various others can be implemented over large number of digits like 64 & 128 or more with consistent delay & lessen complexity. The design in such circuitries is generated through FPGA tools. Modelism software is used for simulation of design while Leonardo Spectrum is used for its synthesis.

This proposed QSD adder works in a better manner than standard binary adders while considering the factors like higher number of bits addition & number of gates in a consistent time period. The operational speed will be increased through an efficient design of adder block while performing operations like addition & multiplication. There is around ¼ less space acquired by QSD numbers than the BSD while QSD adder can support more number of gates with further enhancement.

In march 2015 Ms. Priti S. Kapse presented a paper for QSD addition according to them Adders are most commonly used in numerous electronic applications and serves as the basic building block of various arithmetic operations. As we know that the speed of the digital processor mainly depends on the speed of the adders used in the system. System speed can be increased by increasing the speed of addition. Speed of the system is limited by the carry formation and propagation especially when the number of bits are large. In QSD number system , carry propagation chain are eliminated which reduce the computation time substantially, thus enhancing the speed of the machine[2]. Output values in the range from +3 to -3 can be represented by single digit QSD number but when these output values exceeds from the above range more than one QSD digit is required to represent that value. In this two digit QSD number, LSB represents sum bit and MSB represents intermediate carry bit. This intermediate carry propagates from lower significant digit to higher significant digit position and to prevent this propagation QSD number representation is used
In 2015 Bhavya Sree Kotte,et.al [et.al] presented a paper for These days adders are mainly implemented in electronic components like computational devices & digital signal processors. Adders are able to implementing several algorithms such as IIR, FIR etc. In the present electronic components, digital systems have got an important place in routine. The arithmetic functions like addition, subtraction & multiplication has to still deal with some issues like restricted number of bits, complexity of circuit, time delay in propagation. The speed of operation by adders determines the speed of digital processors which have some constraints such as power, speed & area. The carry chain moulds the path of delay incorporated in adder. Binary signed digit numbers implemented in adders help to limit the propagation of carry with more complicated process of addition. Fewer such limitations applied over the system are related to speed of computation that also confines generation & propagation of carry particularly with a hike in number of bits. Hence, it leads to higher complexity & less density of storage. Carry free arithmetic operations are attained through high radix number system like QSD. In provided research, carry propagation chain is eliminated by QSD number system that also lessens the time of computation & also improving speed. QSD adder or Multiplier is the logic circuitries that are designed for implementing high speed arithmetic functions. A high radix based signed digit number system like QSD helps in high information storage density & lower complexity. A high speed & area effective adders & multipliers are applied through this technology. Carry free addition & similar operations are applied over larger digits like 64, 128 or more that can be applied through consistent delay & lower complexity. Xilinx 10.1 is used for simulation & synthesis of design.[3].

IV. CONCLUSION

This review paper discussed the idea of both converters; decimal number to QSD number converter and also QSD number to decimal number converter. By using this higher radix number system such as QSD we can perform the operations on large number of bits with constant delay and less complexity. As technologies are becoming more complex, multivalued logic (MVL) will be the future of circuit design. Hence MVL logic scheme can be a solution for the demand of increasing data storage capability and faster processing.[3]

REFERENCES

[1]. Kothuru.Ram Kumar, P. Venkata Ramana, "Design and Implementation of QSD Adders for Arithmetic Operation ", International Journal Of Professional Engineering Studies , Volume II/Issue 3/JUNE2014.

All Rights Reserved © 2017 IJERECE

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 3, March 2017

[2].Reena Rani, Neelam Sharma, L.K.Singh, "Fast Computing using Signed Digit Number System", IEEE proceedings of International Conference on Control, Automation, Communication and Energy Conservation – 2009, 4th-6th June 2009

[3] Ms. Priti S. Kapse, Dr. S. L. Haridas "design of quaternary adder for high speed applications" International Journal of Science, Technology & Management Volume No 04, Special Issue No. 01, March 2015 ISSN (online): 2394-1537

[4] Shristi Arora, Abhilasha "Review for QSD Number Addition / Subtraction" International Journal of Innovative Science and Research Technology October – 2016

All Rights Reserved © 2017 IJERECE