ISSN (Online) 2456 -1304

International Journal of Science, Engineering and Management (IJSEM)
Vol 3, Issue 4, April 2018

Comparative Analysis of Convolution Encoder Using Booth Algorithm and Vedic Mathematics

[1] Poonam R. Chaudhari, [2] Pravin R. Lakhe, [3] P D.Bhirange
[2][3] Asst. Prof.
[1][2][3] Suresh Deshmukh College of Engg. Wardha

Abstract— **The communication play important role in today's world. Various technique are been adopted to make the communication system more efficient and reliable. This can be achieved by making the channel less noisy and the data to be more resistant to noise. One of the techniques used to avoid the noisy channel is Convolution Encoder. As we know that a convolution encoder is a system where in multiple multiplication is carried out, this encoder can be designed by various method. In present scenario the convolution encoder is being designed using VEDIC Mathematics and BOOTHS Algorithm. A comparative study and analysis using both the method is been done which help in making Application based Convolution Encoder.**

I. INTRODUCTION

Convolutional encoding is one of the forward error correction schemes. Error correction technique plays a very important role in communication systems. The error correction technique improves the capacity by adding redundant information for the source data transmission. It provides an alternative approach to block codes for transmission over a noisy channel. Convolutional codes are characterized by code rate and memory of the encoder (n,k,K). The code rate is typically given as n/k,where n is the input data rate and k is output symbol rate.The memory is called the "constraint length" 'K' where the output is a function of the previous K-1 inputs. Convolutional codes were introduced in 1965 by Peter Elias.Convolutional codes are used extensively in numerous application in order to achieve reliable data transfer ,including digital video, radio, mobile communication and satellite communication. Convolution encoding is a process of adding redundancy to the information sequence which is going to be transmitted over the channel. Redundancy means introducing some extra symbols to the information sequence so that the output bit pattern generated makes the transmitted data more immune to the noise in the channel. A convolution encoder processes the information serially.

In today's digital communications, the reliability and efficiency of data transmission is the most concerning issue for communication channels. Error correction technique plays a very important role in communication systems. The error correction technique improves the capacity by adding redundant information for the source data transmission. In the late 1940's the approach to error correction coding taken by modern digital communications system started with the ground breaking work of Shannon, Hamming and Golay. The theoretical limits of reliable communication were defined by the Shannon while Hamming and Golay were developing the first practical error control schemes. Hamming and Golay codes are categorized as linear block codes. In 1954, a new class of linear block codes named Reed-Muller codes were discovered by Muller. Reed-Muller Codes allowed more flexibility in the size of the code and the number of correctable errors per code word. All communication channels are subject to the additive white gaussian noise (AWGN) around the environment. Forward error correction (FEC) techniques are used in the transmitter to encode the data stream and receiver to detect and correct bits in errors, hence minimize the bit error rate (BER) to improve the performance. RS decoding algorithm complexity is relatively low and can be implemented in hardware at very high data rates. It seems to be an ideal code attributes for any application. However, RS codes perform very poorly in AWGN channel. Due to weaknesses of using the block codes for error correction in useful channels, another approach of coding called convolutional coding had been introduced in 1955.

II. MOST PROBLEM REGARDING SPV SYSTEM

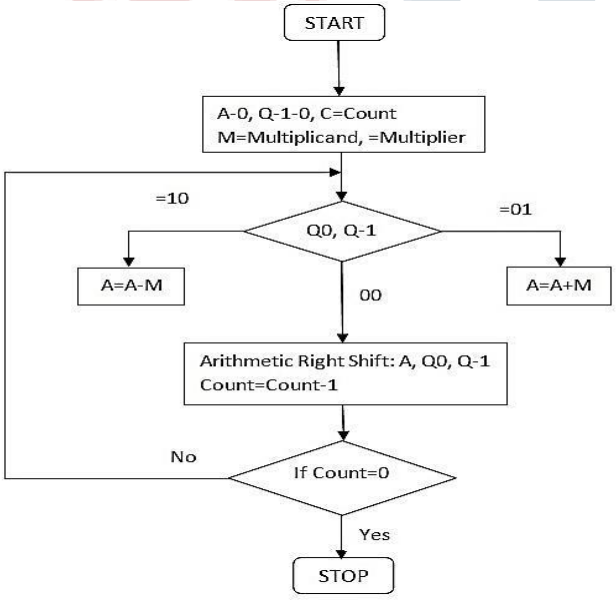
A convolutional code is a type of error-correcting code which differs a lot from block codes. First, the former does not have code words made up of distinct data sections and block sections. Instead, redundant bits are distributed throughout the coded data. Second, the encoder of the former contains memory and the n encoder outputs at any given time unit depend not only on the k inputs at that time unit but also on m previous input blocks. Convolutional codes are sometimes referred as trellis codes. Normally, convolutional encoding is simple, but decoding is much more difficult. Convolutional codes are usually characterized by two parameters and the patterns of n modulo-2 adders. The two important parameters are the code rate and constraint length. The code rate (k/n)

ISSN (Online) 2456 -1304

International Journal of Science, Engineering and Management (IJSEM)
Vol 3, Issue 4, April 2018

where the number of output bits must equal or bigger than the input bits (n_k), is expressed as a ratio of the number of bits into the Convolutional encoder k to the number of channel symbols output by the Convolutional encoder n in a given encoder cycle. To convolutionally encode data, start with m memory registers, each holding 1 input bit. Unless otherwise specified, all memory registers start with a value of 0.The encoder has n modulo-2 adders, and n generator polynomials, one for each adder. An input bit m1 is fed into the leftmost register. Using the generator polynomials and the existing values in the remaining registers, the encoder outputs n bits. The word 'Vedic' is derived from the word 'veda' which means the store-house of all knowledge. There are 16 Sutras in Vedic multiplication in which "Urdhva Tiryakbhyam" has been noticed to be the most efficient one in terms of speed. A large number of high speed Vedic multipliers have been proposed with Urdhva Tiryakbhyam sutra. Vedic multiplier is one of the fastest and low power multiplier. This sutra is based on "Vertically and Crosswise" technique. It makes almost all the numeric computations faster and easier. The advantage of multiplier based on this sutra over the others is that with the increase in number of bits, area and delay increase at a smaller rate in comparison to others.

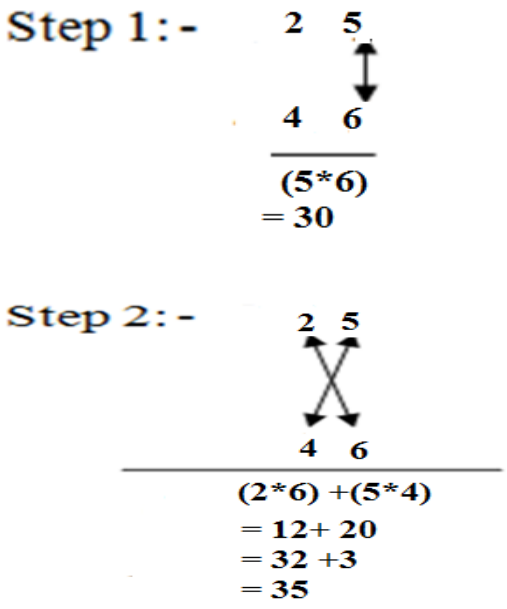
III. BOOTHS ALGORITHM FLOWCHART



BOOTHS Multiplication Example
If 00 then P= Arithmetic Rig
ht Shift
If 11 then P= Arithmetic Right Shift
If 01 then P=P+A
If 10 then P=P+S
Example :- 4*4
m=4=0100 m=- 4 =1100
r=4=0100 r=-4=1100
A= 0100 0000 0
S= 1100 0000 1
P= 0000 0100 0
perform the loop 4 times :
P= 0000 0100 0
Right shift P= 0000 0010 0
P= 0000 0010 0
Right shift P= 0000 0001 0
P=0000 0001 0
P=P+S= 0110 0001 0
Right shift P= 0011 0000 1
P=0011 0000 1
P=P+S=0010 0000 0
Right shift=0001 0000 0
The product is 0001 0000 which is 16.

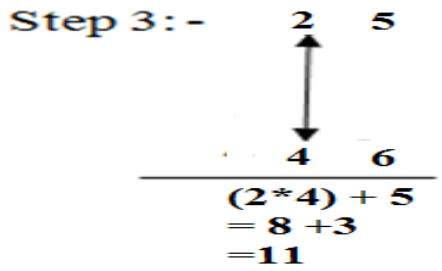
IV. VEDIC ALGORITHM

Consider an example: - A = 25 & B = 46



ISSN (Online) 2456 -1304

International Journal of Science, Engineering and Management (IJSEM)
Vol 3, Issue 4, April 2018



Hence, the answer is 1150

V. OVERALL ANALYSIS OF REVISED WORK

Many of the literature reviewed describes about the Convolution Encoder using various techniques. . There are many techniques and algorithms available for transmission and reception of digital data over noisy channel but Convolution Encoder and Viterbi Decoder are most efficient. It gives improved coding gain and enhanced performance [1]. The bits which are encoded are again sent to the Viterbi Decoder and then the decoded output is obtained [2]. The transmitted sequence is decoded by the Viterbi decoder and the estimated original sequence is produced [3]. The input signal to the convolution encoder is identical to the output signal from the Viterbi decode. So this parallel design of TB and DECODER module meet requirements [4]. All the synthesis and placement and routing are done with ISE foundation from Xilinx and the whole simulation processes are carried out on Modelsim software

VI. PROBLEM DEFINATION AND FORMULATION

Multipliers are key components of many high performance systems such as microprocessors, FIR filters, digital signal processors (DSP) etc. Mostly, many of the researchers concentrated on the design of a 4-bit, 8-bit Booth and Vedic multiplier. I will propose a High Speed; low power Advanced Convolutional Encoder using Booth and Vedic Multiplier to increase the speed of the devices. The main target of this project is to increase the speed of these devices by reducing the delay and power. Convolutional codes are applied in applications that require good performance with low implementation cost. They operate on data stream only, not on static blocks. Convolutional codes have memory that uses previous bits to encode the resultant bits. Convolutional encoder is a finite state machine (FSM), processing information bits in a serial manner, it does not follow parallel processing manner. Thus the generated code is a function of input and the states of the FSM.

VII. OBJECTIVE

The main objective of this research work is to design, synthesis and simulate convolutional encoder using booth and Vedic multiplier. Our target is to increase the speed of this device by reducing the delay and power.
Multiplication is an important fundamental function in many Digital Signal Processing (DSP) applications such as convolutional encoder. Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier. The following are the main objective of this project.
To reduce delay.
To reduce power.
To increase the speed

VIII. PROPOSED METHODOLOGY

The Proposed work is to design of High Speed 16-Bit Convolutional Encoder using Booth and Vedic Multiplier. 16-Bit Convolutional Encoder can be composed of 6-Booth Multiplier / 6-Vedic multipliers and D flip-flops. Following figure shows a proposed block diagram of High Speed 16-Bit Convolutional Encoder using Booth and Vedic Multiplier based on VHDL.

IX. CONCLUSION

The proposed work is likely to achieve the Booth Multiplier, Vedic Multiplier, D Flip-flop and Convolutional Encoder using Booth as well as Vedic Multiplier. Hence Convolutional Encoder using Booth and Vedic Multiplier with high speed is the probable outcome of this research work.

REFERENCES

[1] Bineeta Soreng, Saurabh kumar, Efficient Implementation of Convolution Encoder and Viterbi Decoder, 978-1-4673-4922-2113/$31.00 ©20 13 IEEE / 2013 International Conference on Circuits, Power and Computing Technologies [ICCPCT-2013].

[2] Ms.G.S. Suganya, Ms. G.kavya, RTL Design and VLSI Implementation of an efficient Convolutional Encoder and Adaptive Viterbi Decoder, 978-1-4673-4866-9/13/$31.00 ©2013 IEEE / International conference on Communication and Signal Processing, April 3-5, 2013, India..

[3] V.Kavinilavu, S. Salivahanan et.al, Implementation of

Convolutional Encoder and Viterbi Decoder using Verilog HDL, 978-1-4244-8679-3/11/$26.00 ©2011 IEEE.

[4] Lei -ou Wang , Zhe-ying Li, Design and Implementation of a Parallel Processing Viterbi Decoder Using FPGA 978-1-4244-6936-9/10/$26.00 ©2010 IEEE.

[5] Yin Sweet Wong, et. Al, Implementation of Convolutional Encoder and Viterbi Decoder using VHDL, 978-1-4244-5187-6/09/$26.00 ©2009 IEEE/ Proceedings of 2009 Student Conference on Research and Development (SCOReD 2009), 16-18 Nov. 2009, UPM Serdang, Malaysia.

[6] Hema. S, Suresh BABU. V and Ramesh P, "FPGA Implemcntation of Vitcrbi Dccodcr," Procccdings of thc 6th WSEAS Int. Conf. on Electronics, Hardware, Wireless and Optical Communications, Corfu Island, Grcccc, Fcb. 2007. pp.162-167.

[7] Qing Li, Xuan-zhong Li, Han-hong Jiang and Wen-hao He, "A Hign-spccd Vitcrbi Dccodcr," Fourth Intcrnational Confcrcncc on Natural Computation, 2008, pp. 313-316.

[8] Robert Cypher and C. Bernard Shung, "Generalized Trace-Back Techniques for Survivor Memory Management in the Viterbi Algorithm," Journal of VLSI Signal Proccssing, vol 5, 1993, pp. 85-94

[9] A.J. Viterbi, "Error bounds for convolutional codes and an asymptotically optimum decoding algorithm," ieee transactions on information theory, vol. it-13,april, 1967, pp. 260-269.

[10] Yogita Bansal, Charu Madhu, Pardeep Kaur," High speed vedic multiplier designs-A review", Proceedings of 2014 RAECS UIET Panjab University Chandigarh, 06 – 08 March, 2014.

[11] VHDL Primer by J. Bhaskar.