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A Heuristic One Pass Design and Optimization technique for Reversible Sequential Logic

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***Abstract*—Design of reversible sequential circuits is an engaging area in reversible logic synthesis. The works attempted in the domain is meager. The paper confers an improved implementation for reversible sequential logics using heuristic one-pass design technique of reversible circuits, which is a combination of embedding and synthesis.This strategy is vindicated by adopting the Transformation and KFDD based combinational reversible synthesis algorithms. Adding line optimization approach is applied on synthesized circuits, results in prime implementation cost. Quantum cost and the Transistor cost are taken as the cost functions to measure the quality of the design and the optimization**

***Index Terms*—Reversible logic, Sequential circuits, quantum computing, reversible Synthesis, Optimization**

1. INTRODUCTION

Reversible logic, a new epitome in computing, has recently become a prominent area of research. The reason is the increasing demands for lower power devices. Energy dissipation is reduced if computation is devoid of information loss. Bennett shows in [1] that energy debouch of kTln2 J would not occur if computation is reversible, where K is Boltzmann constant and T, the absolute temperature at which computation is performed. Lot of synthesis approaches for reversible logic, including Transformation based approach[2], BDD based approach[2], ESOP based approach[3] etc., are developed. Logic synthesis for reversible functions differs from traditional logic synthesis. In reversible circuits data is bijectively transformed without losing any original informa- tion.

Most of the researches in the reversible logic concentrate in combinational circuits. Limited attempts have been made in sequential logics owing to the presence of feed back that seemingly violate the rules of logical reversibility. A recent work on synthesis of reversible sequential elements [?]justifies no infraction of laws of reversible logic with feedback. A reversible circuit with feedback is feasible if its transition function remains reversible.

For function realization with reversibility, many synthesizing algorithms[?]etc. have been developed but address the aspects of combinational logic only. The paper derives effective method for designing reversible sequential circuits. We use Heuristic one pass approach [4] as synthesis tool and apply Adding line algorithm[5] for optimizing the circuits.

The paper contemplates the idea of reversible logic in section 2.An outline of TB algorithm for combinational cir cuits is presented in section 3.The previous works done in reversible sequential logic synthesis is reviewed in section 4. Section 5 sketches the proposed synthesis and optimization of some reversible sequential circuits. Comparison results are presented in Section 6. Section 7 concludes the paper with some suggestions for further research.

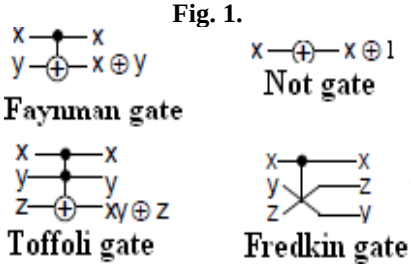
2. PRELIMINARIES

Before presenting reversible sequential circuit synthesis we present some basic concepts regarding reversible logic.

A. Reversible logic

A reversible logic function is one having equal number of inputs & outputs and that maps each possible input vector to a unique output vector. A boolean function which is irreversible can be embedded into a reversible function by means of constant inputs and garbage outputs. A constant input of a reversible function is an input that is set to a fixed value. A garbage output is one which is a don't care for all possible input conditions. According to Shende et al.[6], a gate is reversible if the function it computes is bijective. Most commonly used reversible gates are shown in fig1. and their behavior is listed in fig2.

Fig. 1.



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B. Cost metrics

For addressing various technical constraints in the synthesis stage of reversible circuits, some metrics have been proposed namingly the Cost metrics[7]. Among them, Quantum cost and Transistor cost are selected as means for comparison and optimization criterion in our work. Quantum cost measures the implementation cost of quantum circuits. It is defined as the number of elementary quantum operations needed to realize a reversible gate. Transistor cost, defined as the number of transistors required to realize a reversible gate on CMOS technologies, whose value depends on number of control lines(m) of the gate, and is equal to 8m. Quantum and Transistor costs of a reversible circuit is the sum of the respective costs of its cascaded gates.

gate	behaviour
Not	$(x) \rightarrow (x \oplus 1)$
Feynman	$(x, y) \rightarrow (x, x \oplus y)$
Toffoli	$(x, y, z) \rightarrow (x, y, xy \oplus z)$
swap	$(x, y) \rightarrow (y, x)$
Fredkin	$(x, y, z) \rightarrow (x, z, y)$ *iff* $x = 1$

TABLE II
THE BEHAVIOUR OF COMMONLY USED REVERSIBLE LOGIC GATES.

Fig 2.

3. PREVIOUS WORK

Most of the previous works in the reversible sequential logic is limitted to the design of reversible latches and flip - flops[8][9][10]. Replacement based synthesis , PPRM based synthesis[9] are the two methods existing for revrsible sequen- tial circuit design. The figure(3) shows Reversible flip - flops and their respective augmented tables.

A. Replacement method

The work [9], [10]suggest that sequential reversible circuits be constructed by replacing the gates and flip-flops of tradi- tional logics by their reversible counterparts.This is illustrated by taking the example of mod 8 up counter.Figure (4) shows the traditional circuit for mod 8 up counter with T flip flops. The reversible mod 8 counter after replacement of the T flip- flops and AND gates by their reversible equivalent is depicted in fig(5).

B. Positive Polarity Read Muller (PPRM) Method

This work explains the reversible sequential counter design from the respective transition tables..Here the PPRM coefficients are calculated from the output vector of the table and are realized by reversible gates.PPRM expressions of next state outputs of a mod *N* counter can be written as:

$Qn = qn \oplus Cqn\text{-}1qn\text{-}1q0$ for $n>0$
$Q0 = q0 \oplus C$ for $i=0$

whereQ_n is the next state output and q_n is the present state input. These generalized PPRM expressions allow us to im- plement any up counter directly from reversible gates.The fig- ure(6) shows the reversible implementation of mod 8 counter using PPRM method.

On analyzing it is noticed (table 1-4) that replacement methods[] produce circuits with high realization costs and

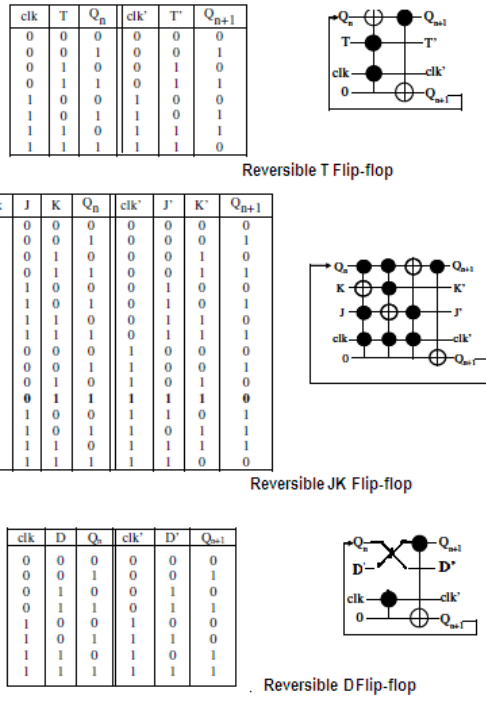

Fig 3

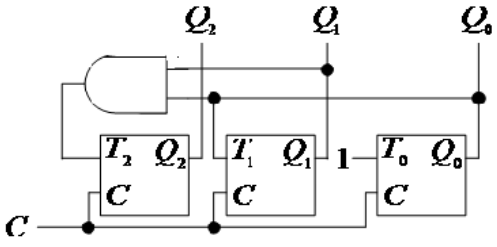

Fig 4

many garbages, while PPRM method yields circuits with lesser realization cost and garbage outputs.But in PPRM method it is needed to generate a PPRM expressions for the next state outputs, which becomes a complex task for sequential circuits other than counters. This limitation forces the need for a general method for synthesizing the reversible sequential circuits. This paper proposes a

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generalized approach to the construction of reversible sequential logics.

4. ALGORITHMS

In this section Transformation based algorithm used in the synthesis of reversible combinational circuits and Adding line algorithm for optimization of synthesized circuit is described.

A. Transformation based algorithm

TB based algorithm[] provides an efficient method for synthesizing reversible logic. The method is based on the basic

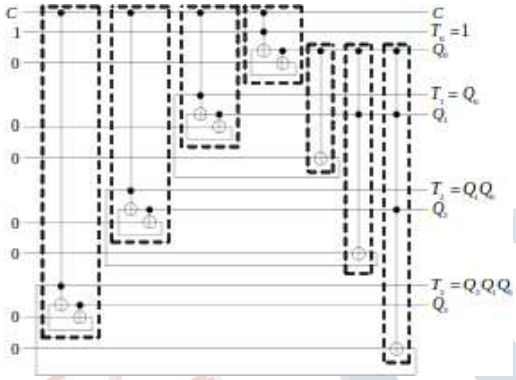

Fig 5.

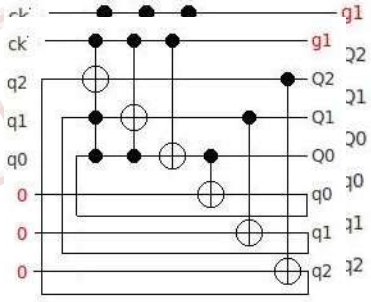

Fig 6.

idea that adding a toffoli gate would not alter the reversibility of a function. The approach follows sequencing of Toffoli gates until input output identity is attained. The algorithm is as follows.

The algorithm:

Input: a reversible specification $f = f 1, , fn$

Output: a circuit composed of toffoli gates which when applied to f produces a unique function

B. Adding line optimization algorithm

Adding line algorithm is an effective approach for optimizing the implementation cost of synthesized reversible logics.The technique is on the basis that extract factors from Toffoli and Fredkin gates in the circuit and extending the circuit by adding lines (helper lines), whose input is set to zero and output is a garbage having don't care value.The algorithm can be employed repeatedly to add more than one helper line and can be iterated to add lines until adding a further line results in no cost reduction.

The algorithm:

Consider a reversible circuit G consisting of the cascade of gates tt_1tt_2 ::: tt_k. Let $C_i$denote the set of control lines for tt_i and let T_i denote the set of target lines for tt_i.

1) Add a single helper line h.
2) Find the highest cost reducing factor across the circuit as follows:

For 1 _ i ≤k ≤

If tti is an MCT or MCF gate and the helper line h is available, i.e. it is not being used by a previously applied factor at this point in the circuit: For every partitioning of Ci into F, Cj with F not empty:

Find the lowest $j>i$

such that i = k or $(F(T_{j+1}))$ = φ i.e. find the next gate tt_j that manipulates one of the lines in F so that the value of the helper line cannot be reused any longer.If the outputs of the circuit are reached use tt_k instead. Determine the cost reduction that would result from applying this factor to all applicable gates between tt_i andtt_j ,including the cost of introducing two instances of the factor gate *MCT* (*F*, *h*). Keep a record of the factor and the gate range that leads to the greatest cost reduction.

3) If no cost reducing factor is found in 2,terminate.
4) Otherwise, apply the best factor found and repeat from step (2) on the revised circuit.

Note: the rightmost *MCT* (*F*, *h*) operating on the helper line is only added if the helper line is going to be used for another factor.

5. PROPOSED DESIGN FOR SYNTHESIS AND OPTIMIZATION OF REVERSIBLE SEQUENTIAL LOGIC

The major portion of the work is mapped out in this section.

We propose a generalized technique to design reversible sequential circuits using the Transformation based synthesis algorithm explained in section III. A simple extension to the TB algorithm applied in combinational logic is performed. The circuit is then optimized with respect to implementation cost. Here the reversible synthesis concentrates on reversible Mod N counters.

A. Transformation based synthesis of Reversible sequential circuits

The method has following major steps :

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Construct the state transition table for desired sequential circuit with, input section including all external data inputs & feed back signals of the circuit at time t and output section having the prime outputs at time t+1.Frame the transition table reversible by embedding the table with constant inputs and garbage outputs(if required).Apply Transformation based synthesis approach to implement the transition table.Use the unit wires (as mentioned by Fredkin [7])for providing proper feedbacks from the next state output to the present state input by making a copy of the next state output using Feynman gate.

B. Optimized - Transformation based synthesisof Reversible sequential circuits

In this method the Adding line optimization technique is applied to the TB based synthezied circuit ,before providing feed back.Optimization is applied only if the cost reducing factor, as mentioned in the Adding line algorithm[], is present. The flow diagram for the proposed optimized synthesis of reversible sequential circuit is outlined in fig(7)

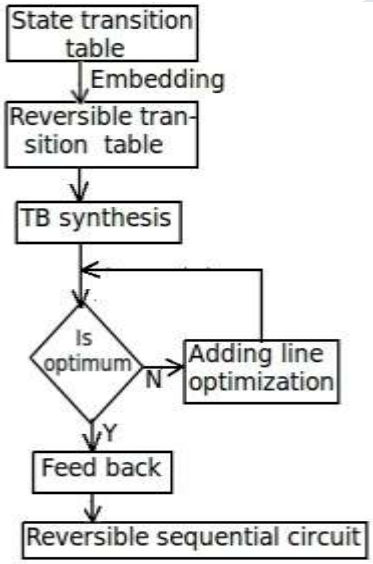

Fig 7

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6. IMPLEMENTATION

The work, carried with the tool Rev kit 1.2.1 on Linux platform. The proposed design can be directly implemented on any sequential logic.But, still Mod N counters were selected for the design because the PPRM synthesis is already implemented on Mod N counter, with which comparison can be made. Design has been carried out for *N* = 2, 4, 8, 16&32. This section gives a description of TB and Optimized TB synthesis of Reversible mod 4 and mod 8 counters.

A. Transformation - based design of Reversible mod N counter

State transition vector of respective counter is undergone transformation based synthesis and appropriate feedback is provided for making reversible sequential counter.

1) Reversible mod 4 counter: The design of reversible mod

4 counter by TB synthesis is depicted in fig (6).The state transition table of mod 4 counter is prepared as the input and is called by the Rev kit in which the TB algorithm is running.The output is generated as the circuit description file as seen in fig.The file can be viewed as its equivalent realized circuit with the help of Rev kit.Cost metrics is calculated for mod 4 counter as QC=2 and TC=16.Where QC is the Quantum cost and TC ,the Transistor cost.

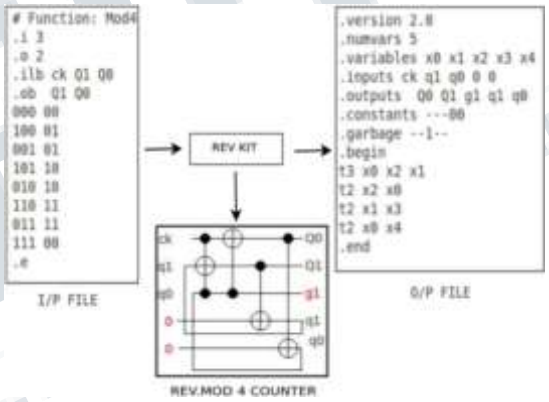

Fig 8

2) Reversible mod 8 counter:

The design is same as that for reversible mod 4 counter.The transition table for mod 8 counter and the equivalent reversible circuit realization by TB method is shown in fig(9).And cost metrics for thi is$QC = 22 TC = 72$

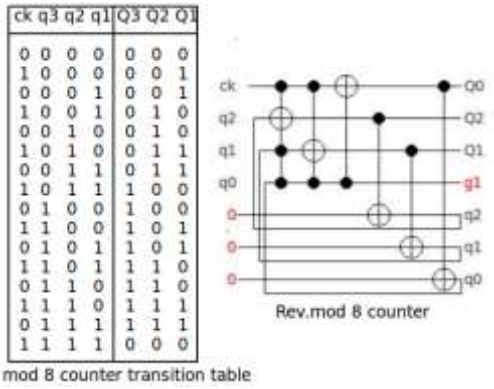

Fig. 9

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B. Optimized Transformation based design of reversible mod N counter

The TB based synthesized circuit from the transition table is checked for optimization by searching the presence of cost reducing factor. , before providing feed back as shown in the fig.Now circuit which is not optimum is undergone adding line optimization.Only then feedback is applied,yielding optimized reversible counter circuit.

1) ***Reversible mod 4 counter:*** Transformation based Reversible mod 4 counter itself is a cost optimized circuit,since no cost reducing factor is present.So Optimized TB based design of reversible mod 4 counter yields the same circuit realization as shown in fig:,and giving no improvement in cost metrics,QC = 2,TC = 16.

2) ***Reversible mod 8 counter:*** The transition table of mod 8 counter shown in fig is undergone TB synthesis. The circuit realized by TB synthesis in fig is seemed to have the cost reducing factor.So it is optimized by applying Adding line algorithm.The feed back is now applied to the resulting circuit to make the reversible counter.On evaluation of cost metrics it is seen that the QC of the optimized reversible mod 8 counter is reduced to 15 from 22,the QC of the Unoptimized one. The whole process discussed is illustrated in the fig(10).

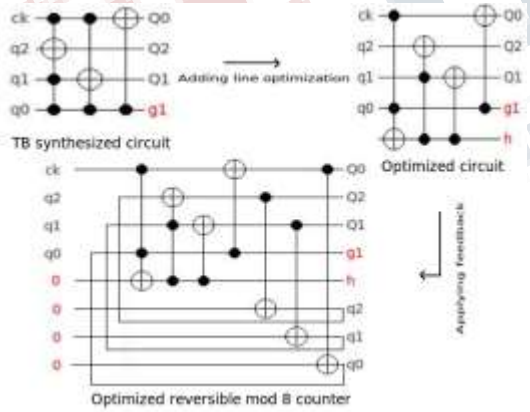

Fig. 10

7. COMPARISON RESULT

Statistics and comparison of our new designs against that proposed in [8,9]is tabulated. We use the Quantum cost and the transistor cost as the cost functions to measure the quality of the design. Optimized - Transformation based design is more cost effective to PPRM and TB based synthesis. The costs obtained for various methods are plotted against mod N and is illustrated in fig(11,12).On analysis it is found that implementation costs of PPRM based and TB based design are equal and is efficient than replacement method.

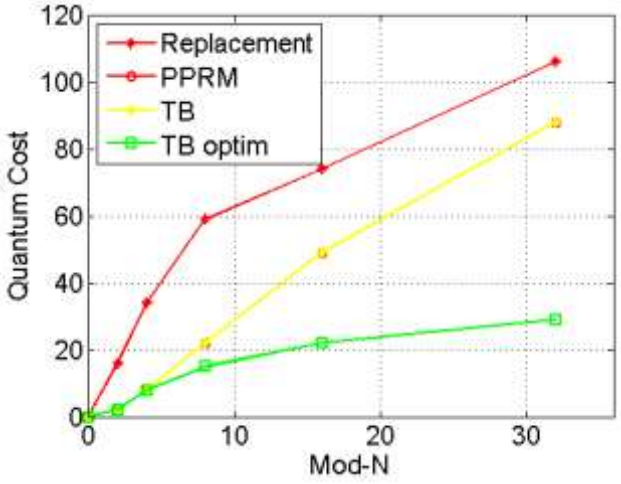

FiG 11

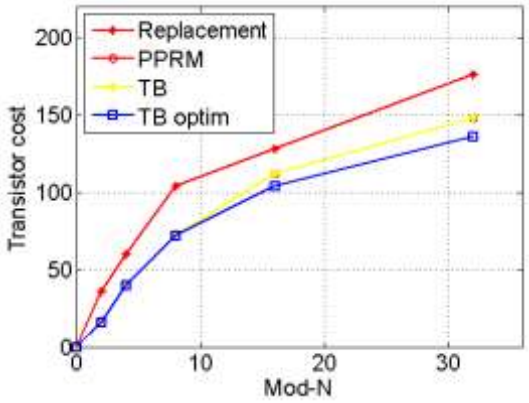

Fig 12

MOD 2 Rev Counter

Method	GC	QC	TC
Replacement method	4	16	36
PPRM method	2	2	16
TB method	2	2	16
TB optimized	2	2	16

MOD 4 Rev Counter

Method	GC	QC	TC
Replacement method	6	34	60
PPRM method	4	8	40
TB method	4	8	40
TB optimized	4	8	40

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MOD 8 Rev Counter

Method	GC	QC	TC
Replacement method	8	59	104
PPRM method	6	22	72
TB method	6	22	72
TB optimized	7	15	72

MOD 16 Rev. Counter

Method	GC	QC	TC
Replacement method	11	74	128
PPRM method	8	49	112
TB method	8	49	112
TB optimized	9	22	104

MOD 32 Rev Counter

Method	GC	QC	TC
Replacement method	13	106	176
PPRM method	10	88	144
TB method	10	88	144
TB optimized	11	29	136

8. CONCLUSION AND FUTURE WORK

The paper endures a few existing works in reversible sequential circuits. Here we proposed a generalized One pass design method for reversible sequential logics with the enhanced Transformation based algorithm. Adding line optimization technique is applied in the synthesized circuits. The Paper derives the conclusion that Transformation based synthesis with adding line optimization technique gives the optimum Quantum cost and Transistor cost

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