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A Comparative Study of Recent Test Methodologies to Test Complex VLSI Circuits

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***Abstract*— Advances in miniaturization technologies have had dramatic impacts on our lives. Radios, computers, and telephones that once occupied large volumes now fit in the palm of a hand. Consequently, it is imperative that the underlying electronic hardware perform correctly and be defect free. However, testing and screening electronic components to requisite "zero defect" standards is extremely challenging. This is due to the defectivity and manufacturing variability inherent in aggressively scaled nanometer IC technologies, and the staggering design complexities. At present, systems –on chips (SOCs) incur 10-15% overheads for design-for-test (DFT) circuitry. Even so, defective parts frequently escape the testing process and cause unacceptable failure in operation. Developing improved test methodologies is a continuing and critical challenge for the microelectronics Industry. This paper compares different testing methodologies and their impact on the complex vlsi circuit is analyzed.**

***Index Terms*— DFT, IC Technologies, SOC, Complex VLSI**

1. INTRODUCTION

Electronics and computing are rapidly transforming society. Be it communication, security, quality of life, health or financial well-being; machines are increasingly being used for making decisions that influence individual and society. Consequently, it is imperative that the underlying electronic hardware perform correctly and be defect free. However, testing and screening electronic components to obtain zero defect standards is extremely challenging.The terminologies Verification, Validation and Testing are used interchangeably and can be confusing at times- at least for entry level engineers. All of these terms does relate to testing of the chip but refers to the same at different stages in a chip design and manufacturing flow. Here is what they really mean. The increased complexity of embedded systems and the reduced access to internal nodes has made it not only more difficult to diagnose and locate faulty components, but also the functions of embedded components may be difficult to measure. Creating testable designs is key to developing complex hardware and/or software systems that function reliably throughout their operational life. Testability can be defined with respect to a fault. A fault is testable if there exists a well-specified procedure (e.g., test pattern generation, evaluation, and application) to expose it, and the procedure is implementable with a reasonable cost using current technologies. Testability of the fault therefore represents the inverse of the cost in detecting the fault. A circuit is testable with respect to a fault set when each and every fault in this set is testable.DFT affects and depends on the methods used for test development, test application, and diagnostics.Most tool-supported DFT practiced in the industry today, at least for digital circuits, is predicated on a *Structural test* paradigm. Structural test makes no direct attempt to determine if the overall functionality of the circuit is correct. Instead, it tries to make sure that the circuit has been assembled correctly from some low-level building blocks as specified in a structural netlist. For example, are all specified logic gates present, operating correctly, and connected correctly? The stipulation is that if the netlist is correct, and structural testing has confirmed the correct assembly of the circuit elements, then the circuit should be functioning correctly. The *fault coverage* is the percentage of detectable faults that are detected by the test, and thus determines how effective the test is.

Fault coverage = Number of detected faults/ Total number of faults in the DUT

2. DESIGN FOR TESTABILITY

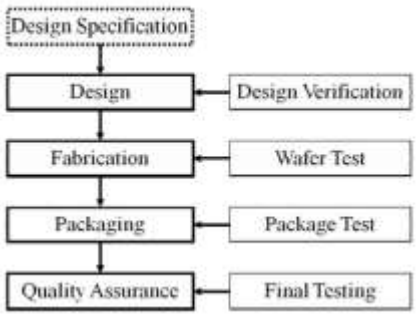

Fig:1 Testing in VLSI Design cycle

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There are many different DFT techniques and each one is used depending on the requirement and the nature of the circuit itself. DFT techniques can be clssified into three major categories:

a.*Ad-hoc DFT techniques* –

Techniques based on designer experience and knowledge e.g. inserting test points at appropriate location. Ad hoc methods are not much widely suited for complex designs.

b. *Scan design* –

Form a scan chain by adding special purpose MUX to test memory elements. Several approaches such full scan or partial scan maybe used.

c. *BIST* –

Built in Self Test - add special purpose circuitry to the chip to generate test patterns, compare the outputs and decide whether the chip works or is defective.

Ad-Hoc Dft Methods

Good design practices learnt through experience are used as guidelines for ad-hoc DFT. SomeImportant guidelines are given below.

A) Things to be followed

Large circuits should be partitioned into smaller sub-circuits to reduce test costs. One of the most important steps in designing a testable chip is to first partition the chip in an appropriate way such that for each functional module there is an effective (DFT) technique to test it. Partitioning must be done at every level of the design process, from architecture to circuit, whether testing is considered or not. Partitioning can be functional (according to functional module boundaries) or physical (based on circuit topology).Partitioning can be done by using multiplexers and/or scan chains.*f* Test access points must be inserted to enhance controllability & observability of the circuit. Test points include control points (CPs) and observation points (OPs). The CPs is active test points, while the OPs are passive ones. There are also test points, which are both CPs and OPs. Before exercising test through test points that are not PIs and POs, one should investigate into additional requirements on the test points raised by the use of test equipments. Circuits (flip-flops) must be easily initializable to enhance predictability. A power-on reset mechanism controllable from primary inputs is the most effective and widely used approach. Test control must be provided for difficult-to-control signals.

Automatic Test Equipment (ATE) requirements such as pin limitation, tri-stating, timing resolution, speed, memory depth, driving capability, analog/mixed-signal support, internal/boundary scan support, etc., should be considered during the design process to avoid delay of the project and unnecessary investment on the equipments. Internal oscillators, PLLs and clocks should be disabled during test. To guarantee tester synchronization, internal oscillator and clock generator circuitry should be isolated during the test of the functional circuitry. The internal oscillators and clocks should also be tested separately.

Analog and digital circuits should be kept physically separate. Analog circuit testing is very much different from digital circuit testing. Testing for analog circuits refers to real measurement, since analog signals are continuous (as opposed to discrete or logic signals in digital circuits). They require different test equipments and different test methodologies. Therefore they should be tested separately.

B) Things to be avoided

Asynchronous (unlocked) logic feedback in the circuit must be avoided.A feedback in the combinational logic can give rise to oscillation for certain inputs. Since no clocking is employed, timing is continuous instead of discrete, which makes tester synchronization virtually impossible, and therefore only functional test by application board can be used.Monostables and self-resetting logic should be avoided. A monostable (one-shot) multivibrator produces a pulse of constant duration in response to the rising or falling transition of the trigger input. Its pulse duration is usually controlled externally by a resistor and a capacitor (with current technology, they also can be integrated on chip).One-shots are used mainly for 1) pulse shaping, 2) switch-on delays, 3) switch-off delays,4) signal delays. Since it is not controlled by clocks, synchronization and precise duration control are very difficult, which in turn reduces testability by ATE. Counters and dividers are better candidates for delay control.

Redundant gates must be avoided.

High fan in/fan out combinations must be avoided as large fan-in makes the inputs of the gate difficult to observe and makes the gate output difficult to control. Gated clocks should be avoided. These degrade the controllability of circuit nodes. The above guidelines are from experienced practitioners. These are not complete or universal. In fact, there are drawbacks for these methods:

- There is a lack of experts and tools.
- Test generation is often manual
- This method cannot guarantee for high fault coverage.

It may increase design iterations.

- This is not suitable for large circuits

3. SCAN DESIGN APPROACHES FOR DFT

A) Objectives of Scan Design

Scan design is implemented to provide controllability and observability of internal state.Variables for testing a circuit It is also effective for circuit partitioning. A scan design

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with full controllability and observability turns the sequential test problem into a combinational one.

B) Scan Design Requirements

Circuit is designed using pre-specified design rules. Test structure (hardware) is added to the verified design. One (or more) test control (TC) pin at the primary input is required. Flip-flops are replaced by scan flip-flops (SFF) and are connected so that they behave as a shift register in the test mode. The output of one SFF is connected to the input of next SFF. The input of the first flip-flop in the chain is directly connected to an input pin (denoted as SCANIn), and the output of the last flipflop is directly connected to an output pin (denoted as SCANOUT). In this way, all the flip-flops can be loaded with a known value, and their value can be easily accessed by shifting out the chain. Figure 39.1 shows a typical circuit after the scan insertion operation. Input/output of each scan shift register must be available on PI/PO. Combinational ATPG is used to obtain tests for all testable faults in the combinational logic. Shift register tests are applied and ATPG tests are converted into scan sequences for use in manufacturing test.

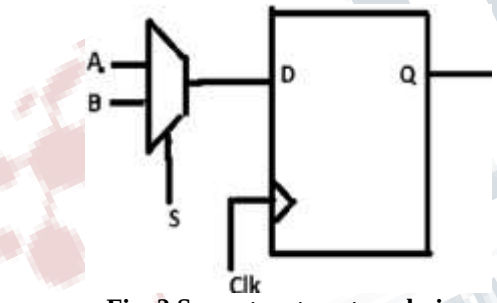

Fig. 2 Scan structure to a design

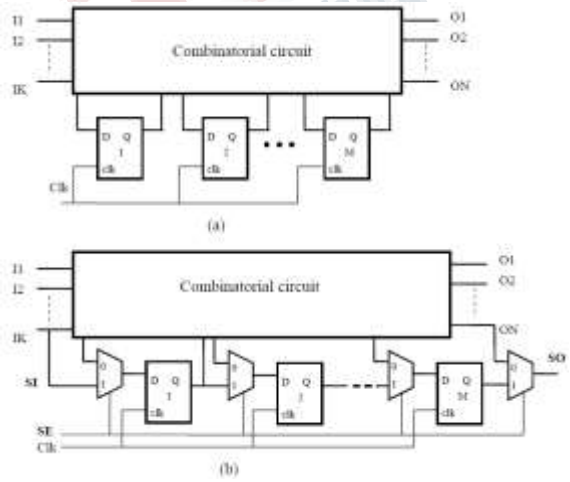

Fig 3:Scan-Path Design

Figure shows a scan structure connected to design. The scan flip-flips (FFs) must beinterconnected in a particular way. This approach effectively turns the sequential testing problem into a combinational one and can be fully tested by compact ATPG patterns. Unfortunately, there are two types of overheads associated with this technique that the designers care about very much. These are the hardware overhead (including three extra pins, multiplexers for all FFs, and extra routing area) and performance overhead.

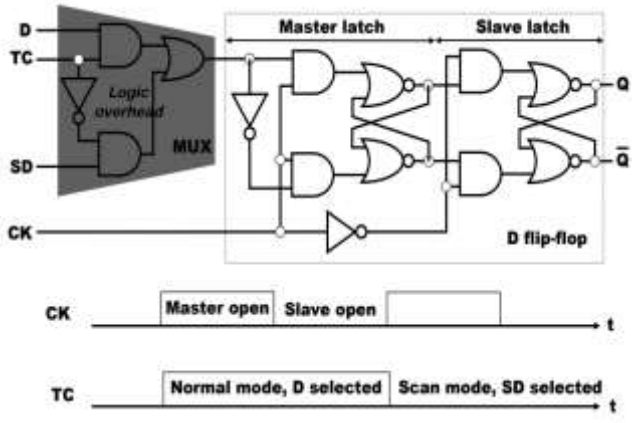

Fig 4:Scan Flip Flop

A) Scan Design Rules

Only clocked D-type master-slave flip-flops for all state variables should be used. At least one PI pin must be available for test. It is better if more pins are available. All clock inputs to flip-flops must be controlled from primary inputs (PIs). There will be no gated clock. This is necessary for FFs to function as a scan register. Clocks must not feed data inputs of flip-flops. A violation of this can lead to a race condition in the normal mode.

B) Scan Overheads

The use of scan design produces two types of overheads. These are area overhead and performance overhead. The scan hardware requires extra area and slows down the signals. IO pin overhead: At least one primary pin necessary for test. Area overhead:
Gate overhead = [4 nsff/(ng+10nff)] x 100%, where ng = number of combinational gates;
nff = number of flip-flops; nsff = number of scan flip-flops;
For full scan number of scan flip-flops is equal to the number of original circuit flip-flops.
Example: ng = 100k gates, nff = 2k flip-flops, overhead = 6.7%.

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For more accurate estimation scan wiring and layout area must be taken into consideration. Performance overhead: The multiplexer of the scan flip-flop adds two gate-delays in combinational path. Fanouts of the flip-flops also increased by 1, which can increase the clock period.

4. BOUNDARY SCAN METHOD

Boundary scan is a method for testing interconnects (wire lines) on printed circuit boards or sub-blocks inside an integrated circuit. Boundary scan is also widely used as a debugging method to watch integrated circuit pin states, measure voltage, or analyze sub-blocks inside an integrated circuit. The boundary scan architecture provides a means to test interconnects (including clusters of logic, memories, etc.) without using physical test probes; this involves the addition of at least one test cell that is connected to each pin of the device and that can selectively override the functionality of that pin. Each test cell may be programmed via the JTAG scan chain to drive a signal onto a pin and thus across an individual trace on the board; the cell at the destination of the board trace can then be read, verifying that the board trace properly connects the two pins. If the trace is shorted to another signal or if the trace is open, the correct signal value does not show up at the destination pin, indicating a fault.

A)On-chip infrastructure

To provide the boundary scan capability, IC vendors add additional logic to each of their devices, including scan cells for each of the external traces. These cells are then connected together to form the external boundary scan shift register (BSR), and combined with JTAG TAP (Test Access Port) controller support comprising four (or sometimes more) additional pins plus control circuitry.Some TAP controllers support scan chains between on-chip logical design blocks, with JTAG instructions which operate on those internal scan chains instead of the BSR. This can allow those integrated components to be tested as if they were separate chips on a board. On-chip debugging solutions are heavy users of such internal scan chains.

These designs are part of most Verilog or VHDL libraries. Overhead for this additional logic is minimal, and generally is well worth the price to enable efficient testing at the board level.

For normal operation, the added boundary scan latch cells are set so that they have no effect on the circuit, and are therefore effectively invisible. However, when the circuit is set into a test mode, the latches enable a data stream to be shifted from one latch into the next. Once a complete data word has been shifted into the circuit under test, it can be latched into place so it drives external signals. Shifting the word also generally returns the input values from the signals configured as inputs.

B)Test mechanism

As the cells can be used to force data into the board, they can set up test conditions. The relevant states can then be fed back into the test system by clocking the data word back so that it can be analyzed.

By adopting this technique, it is possible for a test system to gain test access to a board. As most of today's boards are very densely populated with components and tracks, it is very difficult for test systems to physically access the relevant areas of the board to enable them to test the board. Boundary scan makes access possible without always needing physical probes.

In modern chip and board design, Design For Test is a significant issue, and one common design artifact is a set of boundary scan test vectors, possibly delivered in Serial Vector Format (SVF) or a similar interchange format.

C)JTAG test operations

Devices communicate to the world via a set of input and output pins. By themselves, these pins provide limited visibility into the workings of the device. However, devices that support boundary scan contain a shift-register cell for each signal pin of the device. These registers are connected in a dedicated path around the device's boundary (hence the name). The path creates a virtual access capability that circumvents the normal inputs and provides direct control of the device and detailed visibility at its outputs.[3] The contents of the boundary scan are usually described by the manufacturer using a part-specific BSDL file.

Among other things, a BSDL file will describe each digital signal exposed through pin or ball (depending on the chip packaging) exposed in the boundary scan, as part of its definition of the Boundary Scan Register (BSR). A description for two balls might look like this:

```
"541 (bc_1,              *, control, 1)," &
  "542 (bc_1,      GPIO51_ATACS1, output3, X,   541,
1,  Z)," &
  "543 (bc_1,      GPIO51_ATACS1,   input, X)," &
  "544 (bc_1,              *, control, 1)," &
  "545 (bc_1,      GPIO50_ATACS0, output3, X,   544,
1,  Z)," &
  "546 (bc_1,      GPIO50_ATACS0,   input, X)," &
```

That shows two balls on a mid-size chip (the boundary scan includes about 620 such lines, in a 361-ball BGA package), each of which has three components in the BSR: a control

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configuring the ball (as input, output, what drive level, pullups, pulldowns, and so on); one type of output signal; and one type of input signal.
There are JTAG instructions to SAMPLE the data in that boundary scan register, or PRELOAD it with values.

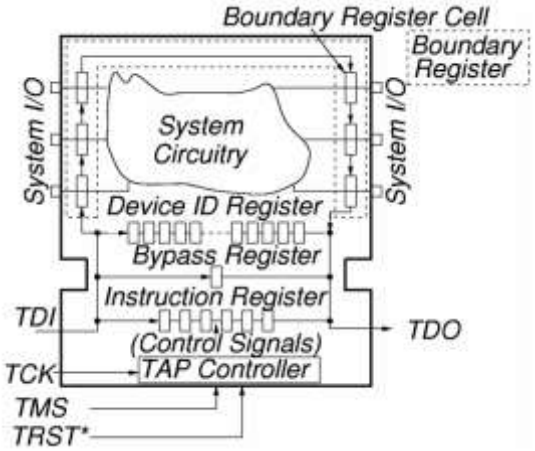

Fig 5: System Test Logic

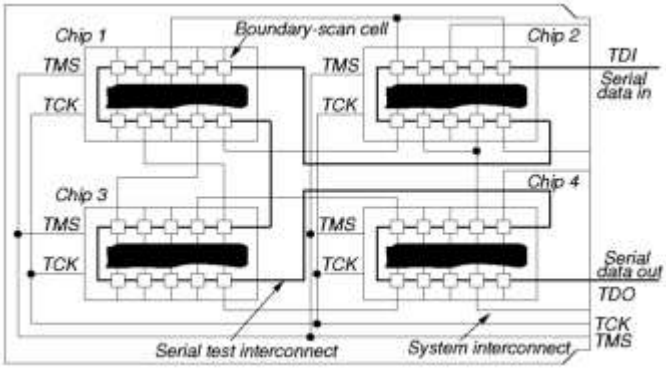

Fig 6: Serial Board Scan

During testing, I/O signals enter and leave the chip through the boundary-scan cells. Testing involves a number of test vectors, each of which drives some signals and then verifies that the responses are as expected. The boundary-scan cells can be configured to support external testing for interconnection between chips (EXTEST instruction) or internal testing for logic within the chip (INTEST instruction).

5. BUILT IN SELF TEST

A built-in self-test (BIST) or built-in test (BIT) is a mechanism that permits a machine to test itself. Engineers design BISTs to meet requirements such as:

- high reliability
- lower repair cycle times

or constraints such as:

- limited technician accessibility
- cost of testing during manufacture

The main purpose of BIST is to reduce the complexity, and thereby decrease the cost and reduce reliance upon external (pattern-programmed) test equipment. BIST reduces cost in two ways:

1. reduces test-cycle duration
2. reduces the complexity of the test/probe setup, by reducing the number of I/O signals that must be driven/examined under tester control.

Both lead to a reduction in hourly charges for automated test equipment (ATE) service.

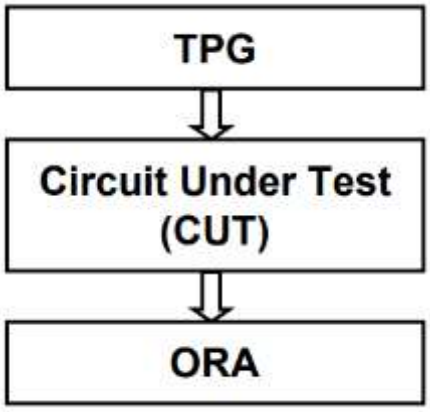

Fig: 7 BIST Architecture

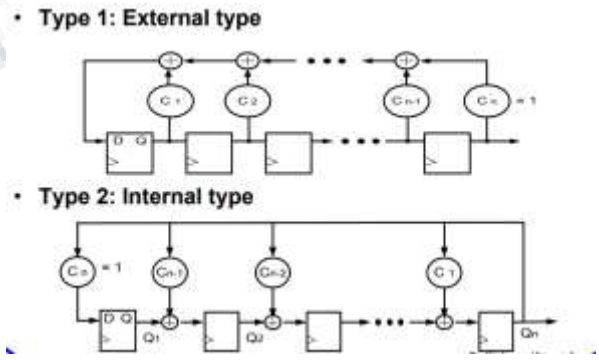

Fig: 8 Two types of LFSR

A sequence of binary numbers can be represented using a generation function (polynomial) • The behavior of an LFSR is determined by its initial "seed" and its feedback coefficients, both can be represented by polynomials. If period p of sequence generated by an LFSR is , then it is a maximum length sequence The characteristic polynomial associated with a maximum length sequence is a primitive polynomial.

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A) Integrated circuit manufacturing

Built-In-Self-Test is used to make faster, less-expensive integrated circuit manufacturing tests. The IC has a function that verifies all or a portion of the internal functionality of the IC. In some cases, this is valuable to customers, as well. For example, a BIST mechanism is provided in advanced fieldbus systems to verify functionality. At a high level this can be viewed similar to the PC BIOS's power-on self-test (POST) that performs a self-test of the RAM and buses on power-up.

B) Computers

The typical personal computer tests itself at start-up (called POST) because it's a very complex piece of machinery. Since it includes a computer, a computerized self-test was an obvious, inexpensive feature. Most modern computers, including embedded systems, have self-tests of their computer, memory and software.

C) Unattended machinery

Unattended machinery performs self-tests to discover whether it needs maintenance or repair. Typical tests are for temperature, humidity, bad communications, burglars, or a bad power supply. For example, power systems or batteries are often under stress, and can easily overheat or fail. So, they are often tested.

Often the communication test is a critical item in a remote system. One of the most common, and unsung unattended system is the humble telephone concentrator box. This contains complex electronics to accumulate telephone lines or data and route it to a central switch. Telephone concentrators test for communications continuously, by verifying the presence of periodic data patterns called frames (See SONET). Frames repeat about 8,000 times per second.

Remote systems often have tests to loop-back the communications locally, to test transmitter and receiver, and remotely, to test the communication link without using the computer or software at the remote unit. Where electronic loop-backs are absent, the software usually provides the facility. For example, IP defines a local address which is a software loopback (IP-Address 127.0.0.1, usually locally mapped to name "localhost").

Many remote systems have automatic reset features to restart their remote computers. These can be triggered by lack of communications, improper software operation or other critical events. Satellites have automatic reset, and add automatic restart systems for power and attitude control, as well.

D) Medicine

Medical devices test themselves to assure their continued safety. Normally there are two tests. A power-on self-test (POST) will perform a comprehensive test. Then, a periodic test will assure that the device has not become unsafe since the power-on self test. Safety-critical devices normally define a "safety interval", a period of time too short for injury to occur. The self test of the most critical functions normally is completed at least once per safety interval. The periodic test is normally a subset of the power-on self test.

E) Military

One of the first computer-controlled BIST systems was in the U.S.'s Minuteman Missile.[*citation needed*] Using an internal computer to control the testing reduced the weight of cables and connectors for testing. The Minuteman was one of the first major weapons systems to field a permanently installed computer-controlled self-test.

6. SUMMARY

Adherence to design guidelines and testability improvement techniques with little impact on performance and area. vendors of design for testability are providing multiple solutions for reducing the increasing test costs substantially. Somany solution options always pose tough choices for the design and test teams. Now a days there are two major options to choose from when confronted with test costreduction problem. Method one is to incorporate test generation and response-capture circuitry onthe chip and the other is generation of extremely compact test patterns. However,Scan is the most popular DFT Technique.Rule based design,Automated DFT hardware insertion,High fault coverage,helpful in diagnosis,Scan testable modules are easily combined into large scan testable systems.

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