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High Performance Pipelined FFT Processor for DAB Receiver

[1] Sindhu T V,[2]Rachana M K, [3]Suvitha P S , [4]Anigha Johnson
[1][2][3][4] Assistant Professor(IESCE)

Abstract: - **With the upcoming fourth generation wireless systems and convergence of multiple radio standards into a single terminal, building blocks are needed that can be configured for computing various algorithms used in different standards. Given these trends and requirements, we require a circuit-sharing design for the DAB receiver to integrate the FFT (fast Fourier transform) and IMDCT (inverse modified discrete cosine transform) operations into the same functional circuit. The proposed technique reduces hardware overhead, enhances circuit efficiency and significantly reduces the cost of DAB receivers.**

This project proposes another alternative design named the circuit-sharing pipeline design (CSPD) using a single processor with a pipeline scheme to combine two functions, FFT and IMDCT, into the same circuit. The proposed method will reduces the required FPGA chip area and cost of DAB receivers. Analyzing the existing relationship among IMDCT, DCT (discrete cosine transform) and FFT, the IMDCT function can be replaced using a FFT function. The arithmetic unit in the FFT processor can be significantly reduced due to employing the pipeline scheme. Consequently, the circuit redundancies in the IMDCT and FFT functions can be easily eliminated to allow exploitation of the decreased chip area. Results of this proposed architecture demonstrate that the design can provide advantages such as low gate count and small memory size in the DAB receiver.

Index Terms— FFT,IMDCT,CSPD,OFDM

1. INTRODUCTION

DAB (digital audio broadcasting), a digital radio system designed to replace analog radio systems such as FM or AM radios, can provide high-quality audio and allow superior reception in cars or on portable radios beyond that possible with FM radios. DAB integrates two digital technologies to create an efficient and reliable radio broadcast system. First, the masking pattern adopts universal subband integrated coding and multiplexing (MUSICAM) and Motion Picture Expert Group (MPEG) Audio layer II, a compression system that decreases the vast amount of digital information required for broadcasting. The second technology, OFDM (orthogonal frequency division multiplexing) guarantees that signals are received reliably and robustly, even in environments frequently susceptible to interference. Two key factors are required to achieve the goals of rapid growth and successful digital broadcasting development, content diversification and receiver popularity.. The cost of terminal devices must be reduced to encourage digital broadcasting development. This difficulty can be eliminated by applying SOC (System On Chip) technology to combine two or more circuits in an integrated chip.

Many studies have concentrated on implementing the DAB receiver. However, a survey of the previous works shows that these schemes focused separately on either the demodulator or source decoder. Recent investigations have introduced the system on a chip concept, giving designers hope that today's expensive, multi-modular systems can be integrated into a single chip, thus decreasing the system weight, power consumption, size and cost.

To combine the functions into the same chip with small required chip area, in our design a circuit-sharing algorithm is proposed that can combine the FFT operations and IMDCT operations into an integrated circuit. The proposed circuit will be simulated using hardware description language with less storage element. However, in the previous circuit-sharing algorithm, we found that the IMDCT circuit remains idle during 1st to 10th stages, while the FFT circuit continues to execute the remaining FFT stages after the IMDCT/FFT finishes the 0th stage. To further improve DAB receiver performance we intend to propose this idle time for other circuit processes. In this project I propose a feasible approach called circuit-sharing pipeline design (CSPD) which can further reduce the integrated circuit area and enhance the circuit efficiency to lower the DAB terminal equipment cost.

II.CIRCUIT- SHARING PIPELINE DESIGN

To remove the hardware redundancies, this project presents a CSPD scheme that can be applied in the DAB receiver to reduce the integrated-circuit area. The proposed CSPD scheme consists of two parts: circuit-sharing design and pipeline scheme. The goal of circuit-sharing design is to analyse the similarities between FFT and IMDCT operations. The circuit redundancies can be removed in designing an efficient circuit using these similarities. In addition, a pipeline scheme can be used to further design a reduced circuit for FFT and IMDCT operation convergence. The proposed circuit will be developed using the CSPD scheme.

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* Similarity Analysis And Circuit Sharing

-- As analyzed above, the similarities between the FFT-based and IMDCT-based operations are summarized as follows.

Similarity 1: OFDM can be implemented by FFT. Also, IMDCT can be performed using FFT.

Similarity 2: The post multiplication operation of IMDCT, calculated using FFT, is a butterfly operation.

Similarity 3: The twiddle factors in FFT operation, IMDCT operation and the post IMDCT multiplication can be accessed from the same ROM.

According to these similarities We design the two FFT functions used for OFDM and IMDCT in the same chip including:

1) A single 2048-point FFT processor is applied to process the FFT functions in OFDM and IMDCT function in audio decoder.

2) A single 512-coefficients twiddle ROM is applied for operation of OFDM, IMDCT and post-multiplication.

3) A synthesis filter flow with a data reordering is designed for IMDCT performed by FFT-based operation,

III. MODIFIED PIPELINE SCHEME

This project will use a modified pipeline scheme to speedup the proposed FFT processor. The modified pipeline scheme applied to the FFT processor uses only one multiplier, one adder and one subtractor to realize the FFT and IMDCT functions. Thus, the FFT processor has the advantages of high integration and low gate-count.

IV.PROPOSED ARCHITECTURE

A. Introduction

The chipset area must be reduced to further lower the cost of the DAB receiver. Based on the CSPD scheme in Section II, a modified FFT processor has been devised to implement OFDM and IMDCT in the DAB receiver. Fig. 2 shows how the connection between the various function units in the proposed modified FFT processor. The architecture comprises a single DIF (Decimation in frequency) radix-2 butterfly process element (PE),a control unit, an interface unit, three dual-port RAM and a twiddle coefficient ROM. The complex input data is stored in the OFDM RAM for later reference by PE. The PE contains the arithmetic unit and other circuitry such as multiplexer and pipelined register to perform the FFT and IMDCT functions with a pipeline scheme. To process the FFT and IMDCT functions the twiddle coefficients stored in ROM and the complex input data stored in RAM are fed to the PE for FFT butterfly operation computation.

The memory access for these operations is coordinated by the control unit and the interface unit. The control unit includes an address generation unit (AGC) and a ROMsharing unit. The goal of the AGC is to generate the RAM and the ROM address in the OFDM and IMDCT mode. The ROM sharing design is proposed to provide the twiddle coefficients for the FFT operation computations in the OFDM and IMDCT mode with a single ROM. The interface unit serves as an arbiter for controlling surrounding units such as an AGC and ROMsharing unit to specify the FFT operation mode—whether it requires the 32-point FFT calculation or 2048-point FFT calculation. That is, the interface unit decides which FFT operation mode will be computed in the proposed circuit. Through all these related units operating together, the results are sent back to RAM for output.

B. Design of Butterfly Process Element

The N-point Discrete Fourier Transform (DFT) of a sequence is given by

$$X(n) = \sum_{k=0}^{N-1} s(k) W_N^{nk}; \quad n = 0, 1, \ldots, N-1 \qquad \text{------ (6)}$$

where $W_N = e^{-j(2\pi/N)}$ Brute force evaluation of (6) needs N2 multiplications N x (N-1) and addition computations. By employing FFT, the computational complexity can be reduced to a number in N x log N.

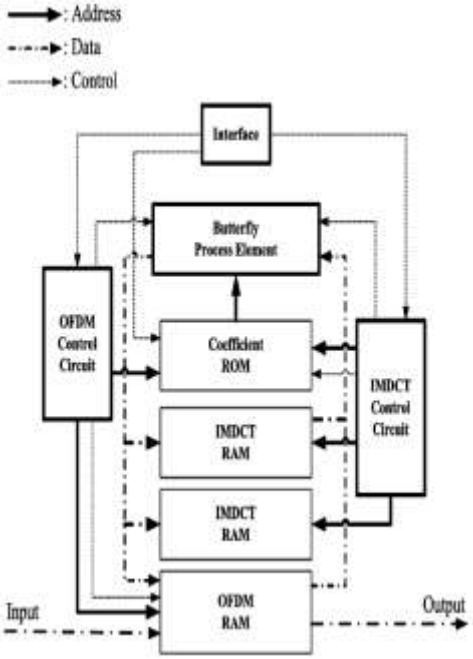

Fig. 2. Block diagram of the proposed modified FFT processor.

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If the number of sampled points is a power of the radix, then the DFT can be measured using a radix- FFT algorithm. In this situation, the N-point DFT can be reduced into a set of recursively related -point transforms. By considering the necessary chip area, this investigation employs the single process architecture with radix-2 for the implementation of a DAB receiver. For the single process implementation, we need 2N X logN memory accesses to calculate one -point FFT operation. This is the major bottleneck for fast FFT computation. Therefore, the pipeline architecture was used on a single process to lower the cycle number of butterfly calculation and increase the memory bandwidth.

This investigation adopts the in-place mode for the design of FFT-based processor to decrease the hardware requirement. The proposed CSPD approach can conduct three-mode operations including: 1) 2048-point FFT butterfly operations in the OFDM mode; 2) 32-point FFT butterfly operations in the IMDCT mode, and 3) 32-point FFT butterfly operations in the post-multiplication of IMDCT mode. Since CSPD employs an in-place algorithm, all these results are written to the sameRAM input locations. As illustrated in Fig. 3, an FFT butterfly operation comprises two sets of complex input data (A and B) and one set of complex coefficient data (C), passing a complex addition/subtraction and multiplication, yielding two sets of complex output (C and D). The complete FFT butterfly operation calculation process can be broken down into five steps,. 1) Read two memory locations for , and , and fetch the coefficients for . 2) Perform addition/subtraction of, , , , , and store the result in temporary storage. 3) Perform multiplication of , , , , and store the result in temporary storage. 4) Perform addition of , , and subtraction of , . 5) Write back the results to the same memory locations.

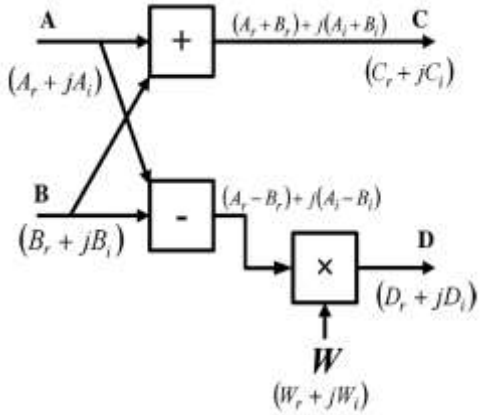

Fig. 3. Butterfly operation.

The butterfly operation presented above can be implemented in a pipeline structure. Fig. 4 illustrates the butterfly operation data path. Table I shows a data path in a pipeline-fashion, in which the major functional units are applied in different cycles resulting in no conflicts from the execution of multiple opera-tions. First, the complex input data are loaded separately into the pipe logic every clock cycle to sustain the rate of the pipeline. Next, subtraction and addition are performed to calculate the operations and at clock cycle 2 (CC2). At CC3, subtraction and multiplication are executed to compute and respectively. Another input datum then enters the PE circuit and begins its eight-cycle execution on CC4. Additionally, and are processed by the multiplier and adder on this clock cycle. At CC5 the operations include: Read, subtraction (SUB), multiplication (MUL), write back (Write). The subtraction is executed as , where the minuend and the subtrahend are derived from the pre-operation results in CC3 and CC4. At the same time, the multiplier performs the operation of on this clock cycle. The output data result, (Cr, Ci) is obtained. The operations proceed to be executed from CC6 to CC8. On CC8, the output data (Dr, Di) is obtained.In the post-multiplication of IMDCT mode, the formula is , which is similar to the FFT butterfly operation, . The post-multiplication can be calculated using the same PE circuit as using for the computation of the butterfly operation by setting the second input data, Y, to zero. The PE can calculate one butterfly operation or one post-multiplication product every four cycles.

C. Interface Unit Design

The interface is the top-level behavioral description for the FFT-based and IMDCT-based operations, and has three main modes: 2048-point FFT calculation for OFDM mode; 32-point FFT calculation with post-multiplication for left-channel IMDCT (LIMDCT) mode, and 32-point FFT calculation with post-multiplication for right-channel IMDCT mode (RIMDCT). The execution sequence of the three modes is decided by the interface based on the feedback from its surrounding units.

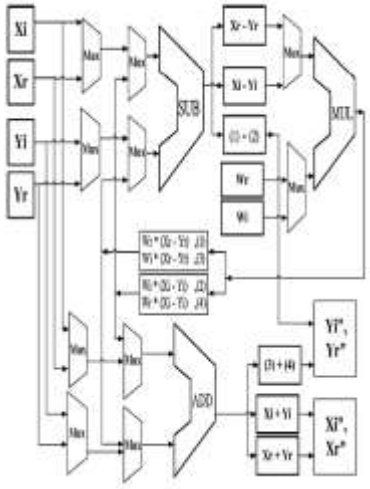

Fig. 4. Block diagram of the proposed process element.

The interface unit creates output signals depending on the above input signals and the current state. The interface unit creates signals including "resetn", "ofdm_imdctn" and "fft_postn" to reset surrounding units to the initial condition and inform AGC of its current mode.

D. ROM-Sharing Design

The aim of the ROM sharing design is to provide a 512-coefficient ROM that can be applied in the OFDM and the IMDCT mode. The ROM sharing design originally needs 1024 coefficients for storing 2048-point FFT twiddle factors. However, by adding extra multiplexes and a sign converter, the 1024 coefficients can be cut to 512 coefficients.

V CONCLUSION

A CSPD to an integrated circuit of FFT operation and IMDCT operation for a DAB receiver was presented in this investigation. To lower the number of butterfly calculation cycles and increase the memory bandwidth we adopted pipeline architecture on a single FFT processor to realize the FFT operation and IMDCT operation. The circuit redundancy in the IMDCT and FFT functions were eliminated using CSPD. Thus, a consumer-economical CSPD solution has been synthesized and proven to be a cost-effective implementation Hopefully, the proposed scheme can be employed to integrate advanced wireless devices such as dual-mode handsets (combination of WLAN and 3G) to remove the circuit redundancy and therefore reduce the chipset area.

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