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A Study on High Performance and Low Power Sram Memories

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***Abstract*— Present day mobile communication devices equipped with large capacity memories in order to fulfill all the multimedia needs of customers. Now a days, design engineer mainly concentrating not only to equip high capacity memories, but also high bandwidth and low power consuming memories. Main advantages of semiconductor memory is that in a very small area it sac store very large data. The SRAM memories are preferred over DRAM because its operation speed is high and large noise margin.In this paper, literature survey on features of various SRAM memory designs was reported.**

***Index Terms*— CMOS, Diode-Gated SRAM, Leakage current, Memories, SRAM, NBTI, MTMOS**

1. INTRODUCTION

RAM (Random-Access Memory) is used in computer for temporary holding the instruction and some data on which CPU process any task. Due to continuous changes in technology less transistor are used for both read and write operation. Now a days large storage in small space possible but in past decade almost 90% area of the embedded chip were occupied by memories. Modern RAM are basically of two types- SRAM (Static RAM), DRAM (Dynamic RAM). When it comes about SRAM, 6T SRAM is generally preferred due to its large noise margin, logic compatibility and high speed of operation.

2. BASIC OF CMOS BASED SRAM OPERATION

Operation of SRAM cell are divided mainly in three states-

A. Standby: If the word line is not asserted, the access transistor m5 and m6 disconnected the cell from the bit line. The two cross coupled inverters formed and it will continue to reinforce each other until they are connected tosupply.

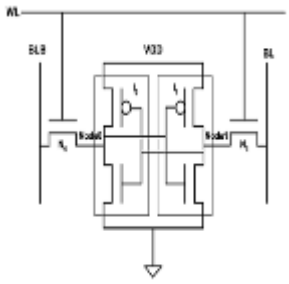

Figure 1: Schematic diagram of 6T SRAM

B. Reading: A SRAM cell consist of 6 transistors is as shown in figure 1. If '1' is stored at Q then its read cycle starts when precharge both bit lines to logic 1, and when word line will be asserted, transistors N0 and N1 will be enable. Now value stored in Q and Qbar will be transferred to bit lines and will discharge with m1 and m5 to logic 0. BL and BLbar will have small voltage difference which sensed through sense amplifier whether it is '1' or '0'. Speed of read operation will be higher if sensitivity will be higher

C. Writing: On applying the written value to the BL, write cycle begins. We can apply 0 or1, whatever we wish to write by inverting the BL. Now we assert WL and latched the stored value.

D. Clock: On the basis of clock SRAM are of two types- single clock SRAM and dual clock SRAM. In single clock SRAM, clock control when input latched at the start of any operation and when at output port, output signal appeared. But in dual clock SRAM, there are different clock for input control and output control. So both types of clock are used in SRAM.

3. LITERATURE SURVEY OF SRAM MEMORIES

J. Abella, X. Vera, and A. Gonzalezanalysed, Since the SRAM cell has cross-coupled inverters, each inverter charges the gate of the PMOS or NMOS device of the other inverter. Therefore, at any given time, one PMOS device will always be in the stress mode. The goal of recovery enhancement is to put the PMOS devices into the recovery mode

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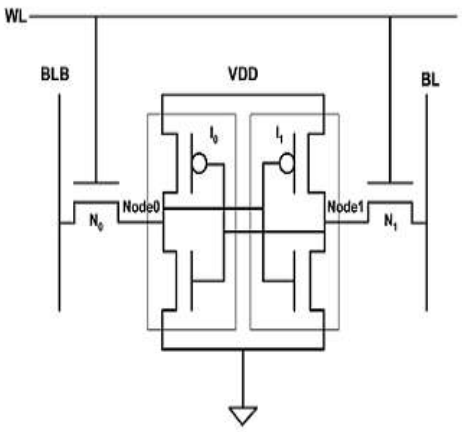

Fig. 2 conventional 6T SRAM Cell

The basic idea behind recovery boosting is to raise the node voltages (Node0 and Node1 in Fig.1) of a memory cell in order to put both PMOS devices into the recovery mode. This can be achieved by raising the ground voltage to the nominal voltage through an external control signal. The modified SRAM cell has the ground connected to the output of an inverter, as shown in Fig.2. CR is the control signal to switch between the recovery boost mode and the normal operating mode. During the normal operating mode, CR has a value of "1", which in turn connects the ground of the SRAM cell to a value of "0." With this connection, the SRAM cell can perform normal read, write, and hold operations. To apply recovery boosting, CR has to be changed to a "0" in order to raise the ground voltage of the SRAM cell to. This circuit configuration puts both PMOS devices in the SRAM cell into the recovery mode. A cell can be put into the recovery boost mode regardless of whether its word line (WL) is high or low. Unlike read and write operations on a cell, putting a cell into the recovery boost mode does not require an access to its word line. The operations of the modified SRAM cell are Shown in Table 1.

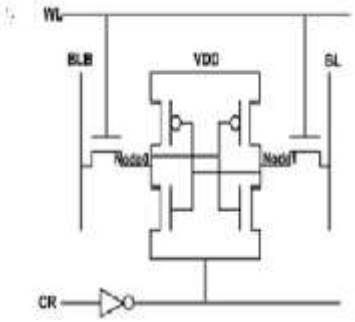

Fig.2 Modified SRAM Cell that Support Recovery Boosting

Table 1 SRAM Cell Operation

CR	WL	BL	BLB	Operation
1	0	X	x	Hold
1	1	1	1	Read
1	1	1	0	Write"1"
1	1	0	1	Write"0"
0	X	X	x	Recovery Boost

However, the drawback of this approach is that it can take a long time to raise both the node voltages to in a high-performance processor that operates at a high clock frequency.This is illustrated in Fig.2 which presents the achieved PMOS gate voltages of a bit cell over time due to recovery boosting.

This problem is solved by adding two extra PMOS access devices. The basic idea is to raise the node voltages and the ground voltage. In the memory cell design, the CR signal serves the same purpose as before. When a value of "0" is input to the CR line to transition the cell into the recovery boost mode, in addition to raising the ground voltage, the two extra PMOS devices connected to the rail are also turned on. Therefore, by raising the ground and connecting the bit cell to, the cell can be transitioned into the recovery boost mode without affecting cells in other rows of the array. Make the extra PMOS devices resilient against NBTI by using these devices are used only when transitioning the cell into the recovery boost mode and not when transitioning to the normal operating mode.

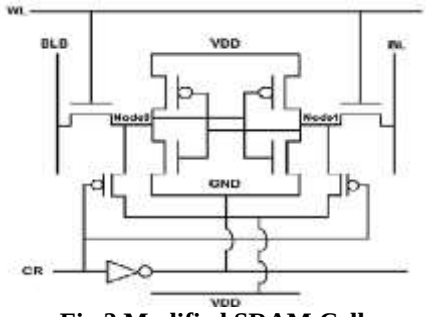

Fig.3 Modified SRAM Cell

There are various ways of incorporating such cells into SRAM arrays, which will discuss shortly. Recovery boosting can be provided at a fine granularity, such as for individual entries/rows of a memory array, or at a coarser granularity, such as for an entire array.We now discuss how the modified high-speed recovery boosting SRAM cells can be used in each of these scenarios and then discuss additional microarchitectural issues related to implementing recovery boosting.

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Achiranshu Garg, and Tony Tae-Hyoung Kim analyzed SRAM Array Structures for better energy efficiency at nominal and low-voltage. They analyzed the energy over different supply levels for array structure of 8T SRAM. As we know energy efficiency is the main concern for most of the ultrapower applications, and in these applications SRAM plays a significant role in energy consumption. In a SRAM arrays structures, there are more rows than columns but in this work a wider SRAM array structure with more columns than rows are used for better energy efficiency at low supply voltage which improve the energy efficiency up to 10% (8kbit) and 38% (64kbit) at same supply voltage. So this analysis revels the fact that at low voltage energy variation in wider array structures is less compared to the traditional tall array structures.

G Rajesh Kumar and K Babulu analysedstatic power can be figured with the assistance of leakage current during the SRAM circuit is in idle state. During this state the access transistors are in cut-off and the bit lines are charged to VDD. The proposed SRAM structure has low VDS and minimum width when standby mode, WL, WR, RD are altogether kept up at 0V rationale zero. The proposed architecture has a sleep transistor which is useful for reducing leakage power when in idle mode. The proposed design has transistors with multiple threshold voltages in order to reduce leakage power. Lower threshold voltage (VTh) devices can reduce power consumption nearly 30 percent when compared with higher threshold voltage circuits.

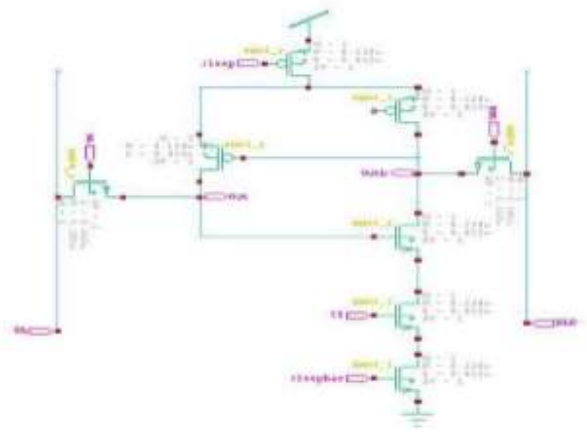

Figure-4.Modified MTCMOS with sleep transistor architecture

Figure-4 shows the modified MTCMOS Static Random Access Memory architecture. All the transistors used to implement logic have low threshold voltage. Low threshold voltage transistors are used for quick switching activity. The transistors connected to the supply node are of high threshold voltage. Sleep transistors with high threshold voltage are used to reduce the leakage current. Low threshold voltage transistors are used in the logic. Pull up and pull down logic blocks are implemented with low threshold voltage transistors. Figure-3 shows the 8X8 SRAM schematic implemented with modified MTCMOS architecture.

CONCLUSION

This paper Review shows the various design method of memory design. Different types of CMOS based memories have been discussed here. Recovery boosting technique in 6T SRAM allows both pMOS devices in the cell to be put into the recovery mode by raising the ground voltage and the bitlineto Vdd. In a SRAM arrays structures, there are more rows than columns but in this work a wider SRAM array structure with more columns than rows are used for better energy efficiency at low supply voltage which improve the energy efficiency up to 10% (8kbit) and 38% (64kbit) at same supply voltage. So this analysis revels the fact that at low voltage energy variation in wider array structures is less compared to the traditional tall array structures. Modified MTCMOS architecture to reduce leakage current.

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